Acquisition for W-CDMA RAKE Receiver System

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Abstract

The RAKE receiver is wildly used to conquer the signal fading in the DS/CDMA (Direct Sequence Code Division Multiple Access) system. To achieve the best performance of the RAKE receiver, an accurate code acquisition is needed in the receiver to estimate the multipath delay in the frequency selective fading environment.

To obtain code acquisition, matched filter (MF) is often used. This paper presents three kinds of matched filter architecture to obtain code acquisition: Parallel type, Serial type and serial-to-parallel type. Each has its pros and cons. We choose proper serial-to-parallel type matched filter to obtain code acquisition according to the consideration of acquisition time and hardware cost.

Introduction

In recent years, the spread spectrum communication systems are more and more important in digital cellular and personal communication networks. In particular, direct sequence code division multiple access (DS/CDMA) has been adopted in third generation cellular standard. This is because direct sequence spread spectrum techniques possess the ability to combat multipath fading, interferences, and to service multiple users over a single frequency channel simultaneously. However, these advantages of DS/CDMA are exploited only if the pseudonoise (PN) code sequence of receiver and the received signal are synchronized. Generally, the process of the synchronization is divided into two steps, acquisition and tracking. Acquisition is the process whereby the received signal code sequence and the replica of the code sequence of the receiver are coarsely aligned, usually within half chip duration. With the successful acquisition, tracking uses a code tracking loop to align the two code sequences more accurately. This paper is mainly focused on acquisition procedure.

RAKE receiver is used in DS/CDMA system to overcome multipath propagation. Acquisition estimates the delays of the received signals, and sets the delay values to RAKE fingers. Generally, to obtain the code acquisition, matched filters (MF) are used. After the received signals passed through the matched filter, the output were the correlation profile. The searcher is required to search the correlation profile, finding the delay of received signals. To evaluate the acquisition performance, the acquisition time and hardware cost are two important issues. This paper is focused on the matched filters design and how to use firmware and hardware to implement acquisition procedure.

RAKE Receiver

RAKE receiver is used in DS/CDMA system to overcome multipath propagation. To evaluate the

performance of the spread spectrum system requires the receiver's phase and frequency and its chip timing to be perfectly synchronized. The synchronization process is called code acquisition. Acquisition is based on the received signal's magnitude of the impulse response of the mobile channel and sets the delay times of the RAKE fingers. The typical RAKE receiver architecture with maximal ratio combining is shown in Figure 1. The matched filter correlates the received signal with local PN code to obtain the delay profile of the multipath fading channel. The searcher is required to search the correlation profile. In the searcher, the threshold is set to select the peak values properly. It must set to obtain the acceptable missing probability false alarm probability. After the acquisition process is completed, the delays are passed to the tracking unit. Finally the maximum ratio combining (MRC) is employed to combine the signals from various paths.

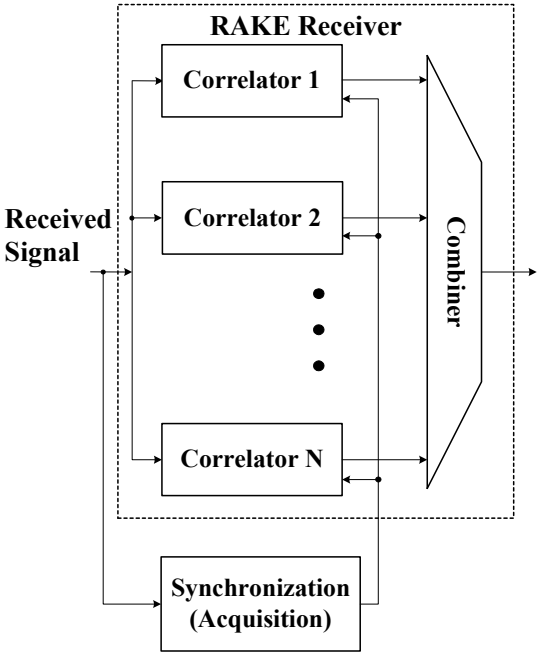

Figure 1. Simplified RAKE receiver with acquisition

Acquisition Architecture

In the WCDMA system, the acquisition is a complicated problem. In the uplink system, signals are received by base station with different propagation delays due to multipath fading channel. Code acquisition process can make the phase of the locally generated PN code within half chip duration of the received signal. The code acquisition process can find the PN offset which has maximum correlation value. The matched filters with different window sizes are used according to the hardware cost and acquisition time that we required. The correlators can be classified as serial or parallel architecture.

The serial-parallel architecture is a compromise between the serial architecture and parallel architecture. It is shown in Figure 2. The serial-parallel architecture is more flexible than the two other architectures. The serial-parallel architecture divides the matched filter (MF) into several sections. The PN code coefficients are loaded in groups. After each group of PN code coefficients is loaded, it provides only a section of the full correlation profile. Until each section of correlation results is summed, the full correlation profile just like that of parallel architecture is achieved.

From the viewpoint of the hardware cost, the matched filter (MF) can be reprogrammed with the next N-chips segment of PN code. It means that the hardware implementation complexity is lower than the parallel architecture.

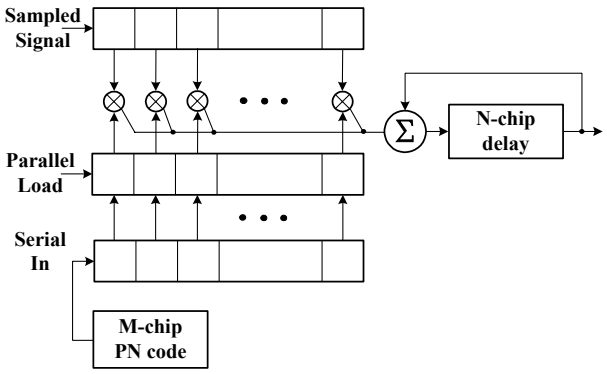

Figure 2. The serial-parallel matched filter architecture

Implementation Feature

- **Task Partition between DSP and FPGA**

We use the FPGA (Field Programmable Gate Arrays) and the DSP (Digital Signal Processor) to implement acquisition function. The principle we decide to put which function onto the DSP or the FPGA is according to the complexity of the algorithm. We put the complex algorithm in the DSP and the regular computation in the FPGA. Besides, the capability of the DSP and the FPGA and the bus traffic of the interface between them are also under consideration. As shown in Figure 3, the functional block in gray is main acquisition function. It provides coarse acquisition result to the tracking unit. The timing resolution of the peak location from acquisition result is in the unit of 1/2 chip. Moreover, the tracking unit can improve the timing resolution to 1/16 chip. We can consider it as fine adjustment of the peak location.

The task partition between the FPAG and the DSP in acquisition function can consider as the FPGA provides the delay profile to the DSP, and the DSP finds the peak location. The reason why the peak searcher is put onto the DSP is that the peak search algorithm is complex and needs more flexibility. It is responsible for finding the peak that it is really caused by the effect of multi-path. Besides, the matched filter suits to be implemented by hardware, because it contains a lot of bit-shifting operation.

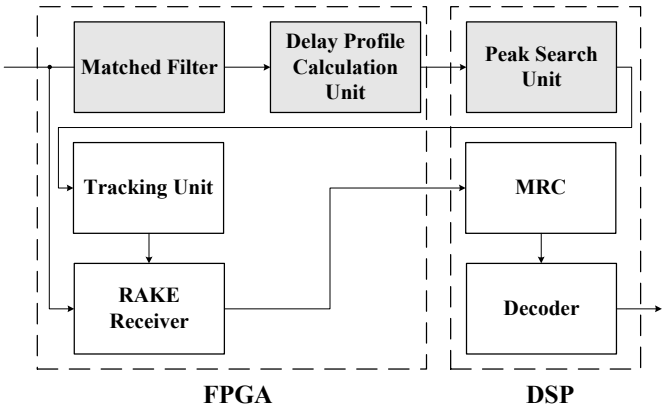

Figure 3. Functional Block Diagram of the Receiver

- **DSP/FPGA Interface**

We use XILINX XCV1000E FPGA and TI TMS320C6201 DSP in the implementation. The capacity of the FPGA is million-gate. The relationship between the DSP and the FPGA can consider as master-slave. We can consider the DSP is the master and the FPGA is the slave. The FPGA receives the primitives and parameters from the DSP. According to the primitives that the DSP gives, the FPGA knows what the computation should be done and uses these parameters to calculate.

The interface between the FPGA and DSP is shown in Figure 4. TI DSP has provided external memory interface, called EMIF. It is an asynchronous memory interface. Because the synchronous interface can avoid some glitch errors and fits to the internal memory in the FPGA, we use simple glue logic to transfer it to the synchronous memory interface. The transferred memory bus is connected to the internal memory bus in the FPGA. Thus DSP can access different internal memory in the FPGA through EMIF. In order to avoid the conflict on the internal bus, the Decoder/Arbiter unit will decide

which internal memory is asserted according to the primitive that the DSP gives.

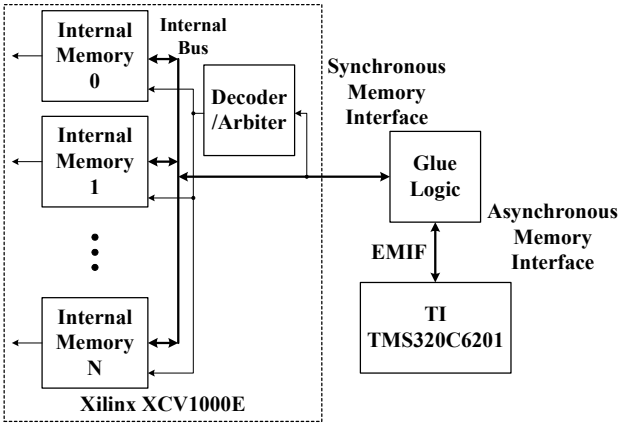

Figure 4. Functional Block Diagram of the DSP/FPGA Interface

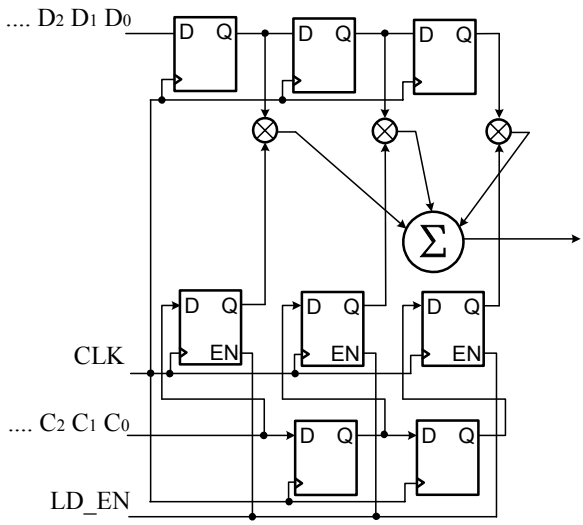

Figure 5. Example of the Circuit Design of the Serial-to-Parallel Type Matched Filter

- **Implementation Architecture of Serial-to-Parallel Type Matched Filter**

As the description above, we decide to use serial-to-parallel type matched filter in our system and implement it in hardware. Figure 5 shows the example of the circuit design of the serial-to-parallel type matched filter. In this example, the tape number is 3. Therefore, the parameter C_0,C_1…C_n is parallel load to the register connected to the multiplier every three clock cycle. We can derive the mathematic from the summation output in the flowing:

Cycle 1 ~ Cycle 2: in the initial state

Cycle 3: $D_0 C_0 + D_1 C_1 + D_2 C_2$

Cycle 4: $D_1 C_0 + D_2 C_1 + D_3 C_2$

Cycle 5: $D_2 C_0 + D_3 C_1 + D_4 C_2$

Cycle 6: $D_3 C_3 + D_4 C_4 + D_5 C_5$

Cycle 7: $D_4 C_3 + D_5 C_4 + D_6 C_5$

Cycle 8: $D_5 C_3 + D_6 C_4 + D_7 C_5$

Cycle 9: $D_6 C_6 + D_7 C_7 + D_8 C_8$

In this architecture, if the tap number increase, the circuit area of the summation function will be large. In the case of WCDMA, the tap number we use is 128. Therefore, there will be 128 multiple results need to be added at one time. The traditional way is using adder tree for summation. But it takes time to process. Therefore, we use inverse typed serial-to-parallel matched filter. The example of the inversed type serial-to-parallel matched filter is shown in Figure 6.

The inversed type matched filter loads the coefficient inversely. In Figure 6, there are three load enable signals. The signal "*LD_EN0*" will be asserted first. After that, the signal "*LD_EN1*" and "*LD_EN2*" will be asserted in order. We can observe a dotted line with arrowhead in the mathematical form. The inversed type matched filter calculates these dotted terms first. For the example of D_2, it calculates the terms "D_2C_0", "D_2C_1" and "D_2C_2". But it will add the term "D_2C_2" first. And the term "D_2C_1" will be latched for one cycle and is added in the next cycle. Therefore, it separates the

summation in different cycle. It can eliminate the huge adder tree in the previous architecture. But it must carefully control the load enable signal in order to make the data be multiplied by the right coefficient.

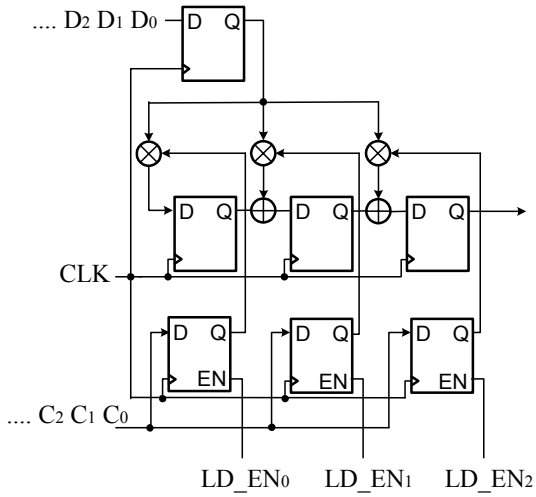

Figure 6. Example of the Circuit Design of the Inversed Type Serial-to-Parallel Type Matched Filter

- **Matched Filter Implementation Result**

Figure 7 shows the delay profile calculated by the matched filter. The test environment includes fading channel which is satisfied the requirement of the 3GPP standard. We can see that the different path caused by the multi-path effect can be easily distinguished.

Table 1 shows all acquisition function implementation result. The first field shows the circuit area overhead of the matched filter in the FPGA. It still has the free area for the rake receiver. The second field shows the peak search algorithm computation loading to the total DSP computing cycles. There are still a lot of the computing cycles can reserve for the complex channel Codec, such like Viterbi Codec and Turbo code Codec.

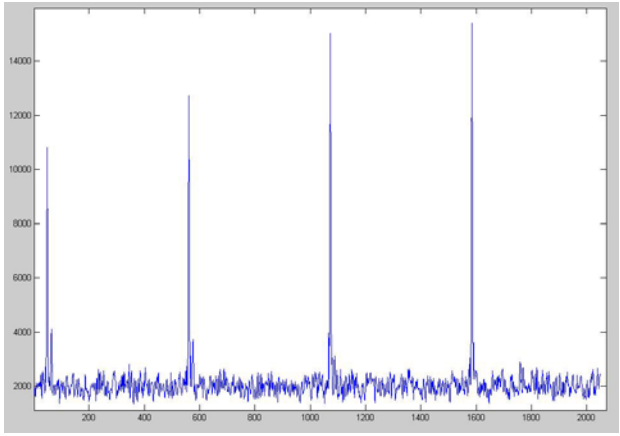

Figure 7. Delay Profile calculated by the Matched Filter

	FPGA	DSP
Area Overhead / Loading	31 %	2.9 %

Table 1. Acquisition Function Implementation Result

Conclusion

This paper introduces the design methodology of acquisition of the WCDMA receiver. Acquisition is important to the spread spectrum system to synchronize the received signals. We use both firmware and hardware in the implementation. The acquisition architecture would be designed for different requirements such as cell size, fading channel and etc. Therefore, under the different consideration, using the hardware combined with firmware can get flexibility.

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