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# A Parallel VLSI Architecture for Two-Dimensional Discrete Periodized Wavelet Transform

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## Abstract

Based on the two-dimensional (2-D) operator correlation algorithm, a novel approach of VLSI architecture design called non-separate architecture is developed to implement the 2-D discrete periodized wavelet transform (DPWT) in this paper. The main features of the architecture are short-time latency, short bit length request, and fast to derive intact octave band components for the purpose of perfect reconstruction. The architecture is composed of three functional units: parallel multipliers, data accumulator, and input data controller. The architecture is in the nature of a parallel processing structure. As a consequence, its parallel modularity makes it well suited for VLSI implementation. A detailed analysis of finite precision performance on the accuracy of 2-D filter coefficients, 2-D DPWT coefficients, and the reconstructed data is also presented in this paper. The overall architecture has been successfully simulated with 21 data bits of Verilog behavioral model simulation to confirm the feasibility.

## I. Introduction

With the significant capability of multi-scale spatial-frequency representation, the 2-D discrete wavelet transform (DWT) developed by Mallat [1-2] has been used in digital image analysis as a powerful tool. The 2-D DWT decomposes a digital image into its different frequency components with octave separation manner, exactly, four sub-images, called octave band decomposition. It is well known that the original image can be reconstructed by the inverse 2-D DWT of the octave band components. In many practical applications such as image coding and compression [3-7], digital image processing [8], scene analysis [9,10], and computer graphics [11,12], they generally require the results of perfect reconstruction (PR) in the inverse process. By this means, the reconstructed image from the inverse 2-D DWT is identical to the original image to the 2-D DWT [4].

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To guarantee the PR result, a finite image in each resolution level (or decomposition stage) should be regarded as a 2-D periodic signal. Otherwise, the information loss will be occurred on each octave image boundary, particularly, when the discrete-time filter length is greater than two. As illustrated an example is shown in Fig.1, a 512x512 image is recursively decomposed until the resolution level of 8x8 image by using the 4-tap Daubechies filter. The result of serious distortion phenomenon is revealed in the upper and left part of the reconstructed image. The periodic assumption implies that PR result of the 2-D DWT can be derived by using the periodized wavelets [13], i.e., the 2-D DPWT.

For real time processing, several VLSI architectures have been proposed to implement the 2-D DWT. Lewis and Knowles [14] proposed an architecture without multipliers to compute the 4-tap Daubechies 2-D DWT. However, this architecture is not suitable for other wavelets. Based on using the RAM transposer, the architecture [15-16] can provide intact octave band components for the purpose of PR result. But, the disadvantage of this architecture is that it needs long latency. Recently, Vishwanath et al. [17] have proposed a systolic-parallel architecture for computing the 2-D DWT with the advantages of area efficiency and short latency (latency=1). The main idea of the architecture design is based on the interleaved computation technology to reduce the latency. In other words, the computations of the various octaves are interspersed into the first octave. The part of systolic architecture is based on the recursive pyramid algorithm [18]. The architecture requires $6d$ multipliers, $2dN$ storage cells, and $N^2 + N$ clock cycles for decomposing an $N \times N$ original image, where $d$ denotes the discrete-time filter length. However, due to lacking the ability of saving the boundary data, the architecture can not provide the inverse 2-D DWT with the PR result. To solve the problem, Truong et al. [19] have proposed a new VLSI architecture to perform the 2-D DPWT process. The architecture design is based on the concept of batch processing. That is, all the octave components in same resolution level are centralized and processed in a specified time interval in which the data sequence can not be interleaved and inserted by the components of other resolution levels. In this architecture, the first stage decomposition is processed during the even-number rows of original image while the other levels are all

concentratedly processed during the odd-number rows. The architecture requires $4d$ multipliers, $(2d-1)N$ storage cells, $d+3$ de-multiplexes, and less than $N^2+N$ clock cycles for decomposing an $N\times N$ original image. However, to deal with the boundary data, the architecture needs a long extra processing time, i.e., $(2^{(k+1)}-1)N$ clock cycles, to derive the last row components in the $k$-th decomposition level, where $k \geq 2$.

Essentially, all the proposed VLSI architectures [14-19] are based on the conventional separate computation, i.e., they use the 1-D filter coefficients in row and column transforms. The conventional architectures have the merit of small area. However, the separate computation usually needs long bit length representation of the 1-D filter coefficients for satisfying the desired finite precision. The long bit length request eventually results in decreasing the area efficiency. Besides, the conventional architectures need complex circuit to deal with the boundary data and long delay time to derive intact octave band components for the PR result.

Employing the modified high pass filter, an operator correlation algorithm is presented to implement the 2-D DPWT process. The modified 2-D DPWT can provide the octave decomposition processes with synchronously handling the boundary data. In addition, the 2-D operator correlation algorithm requesting shorter bit length and less multiplication is superior to the conventional method. Based on the 2-D operator correlation algorithm, a novel parallel-like VLSI architecture is proposed in this paper. The architecture directly using the 2-D filter coefficients is called the non-separate architecture. It is composed of three basic function units: parallel multipliers, data accumulator, and input data controller. The non-separate architecture has the features described as: 1) short-time latency; 2) simple, modular, no input delay, and free to the constrain of decomposition stages; 3) short extra time to derive the last row components, i.e., $kN$ clock cycles for the $k$-th decomposition stage.

In next section, the 2-D operator correlation algorithm for the modified 2-D DPWT implementation is presented. The analysis of finite precision in 2-D DPWT is shown in section III. The non-separate VLSI architecture as well as its simulation result are presented in the section IV. Finally, the section V presents the discussions and conclusion.

## II. Operator Correlation Algorithm for Implementing the 2-D Discrete Periodized Wavelet Transform

Applying the periodized wavelets [13] into the 2-D DWT, the multiresolution decomposition process of a 2-D image is called the 2-D DPWT. With the 2-D DPWT, PR result of the reconstructed image can be derived in the inverse process. However, since the classical 2-D DPWT has time lag between the low pass and the high pass filtering processes, the time lag may cause inconvenience in VLSI architecture design when to deal with the boundary data. In this section, an operator correlation algorithm is presented to perform the modified 2-D DPWT. This algorithm for implementing the 2-D DPWT requires less multiplications and shorter bit length for required accuracy than the separate computation method.

### 2.1. Review of The 2-D DPWT

The periodized wavelets [13] can be defined by a sum of copies of periodically shifted wavelets with reasonable decay. These periodized wavelets form an orthonormal basis in the $L^2([0,1])$ which denotes a 1-D Hilbert space in the interval [0,1]. Let $\phi(x)$ and $\psi(x)$ denote a scaling function and the corresponding mother wavelet function, respectively. For a certain $j \in Z$, the set of translation functions $\{\phi_{j,n}(x)=2^{-j/2}\phi(2^{-j}x-n); n\in Z\}$ constitutes an orthonormal basis for the multiresolution approximation subspace $V_j \subset L^2(R)$. Whereas the set of dilations and translations $\{\psi_{j,n}(x)=2^{-j/2}\psi(2^{-j}x-n);\ j,n\in Z\}$ constitutes an orthonormal basis for $L^2(R)$. For fixed $j$, $W_j$ is the closed subspace with basis $\{\psi_{j,n}(x), n\in Z\}$ and also referred to as the multiresolution approximation subspace. The 1-D periodized scaling and wavelet functions are defined as

$$\tilde{\phi}_{j,n}(x)=\sum_{\ell\in Z}\phi_{j,n}(x+\ell);\quad \tilde{\psi}_{j,n}(x)=\sum_{\ell\in Z}\psi_{j,n}(x+\ell). \quad (1)$$

The corresponding periodic multiresolution approximation subspaces $\tilde{V}_j$ and $\tilde{W}_j$ are spanned by $\tilde{\phi}_{j,n}(x)$ and $\tilde{\psi}_{j,n}(x)$ for $n\in Z$, respectively. Besides, as in the nonperiodic case, subspaces $\tilde{V}_j$ and $\tilde{W}_j$ satisfy the embedded property and orthogonal complement property. It is also shown in [13] that for $j\leq 0$, $\tilde{V}_j$ is spanned by finite functions of $\tilde{\phi}_{j,n}(x)$ with $n\in Z_j \equiv \{0,1,\cdots,2^{-j}-1\}$. A similar result holds for $\tilde{W}_j$ with $\tilde{\phi}_{j,n}(x)$ replaced by $\tilde{\psi}_{j,n}(x)$. For $j\leq 0$, the functions $\tilde{\phi}_{j,n}(x)$ and $\tilde{\psi}_{j,n}(x)$ satisfy the following dilation equations:

$$\tilde{\phi}_{j,n}(x)=\sum_{k=0}^{N-1}\tilde{h}[(k-2n)_N]\tilde{\phi}_{j-1,k}(x), \quad (2)$$

$$\tilde{\psi}_{j,n}(x)=\sum_{k=0}^{N-1}\tilde{g}[(k-2n)_N]\tilde{\phi}_{j-1,k}(x), \quad (3)$$

where $N=2^{-(j-1)}$, $(k-2n)_N$ denotes the residual of $(k-2n)$ mod $N$ and the two coefficients $\tilde{h}[(m)_N]$ and $\tilde{g}[(m)_N]$ have the orthogonal relationship of

$$\tilde{g}[(m)_N]=(-1)^n\tilde{h}[(-n+1)_N]. \quad (4)$$

The 1-D periodized wavelet theory can be extended to the 2-D case [1-2] in which the 2-D DPWT is usually performed by a separable approach. The four corresponding

periodic multiresolution subspaces $\bar{V}_j$, $\bar{W}_j^1$, $\bar{W}_j^2$, and $\bar{W}_j^3$ are spanned by $\Phi_{j,n_1,n_2}(x,y)$, $\Psi^1{}_{j,n_1,n_2}(x,y)$, $\Psi^2{}_{j,n_1,n_2}(x,y)$, $\Psi^3{}_{j,n_1,n_2}(x,y)$ for $n_1, n_2 \in Z$, respectively. For $j<0$, a finite 2-D function $f(x,y) \in \bar{V}_j$, can be approximately represented as

$$\begin{aligned} f(x,y) = \sum_{n_1 \in Z_{j+1}} \sum_{n_2 \in Z_{j+1}} & (SS_{j+1}[n_1,n_2]\, \Phi_{j,n_1,n_2}(x,y) \\ & + SD_{j+1}[n_1,n_2]\, \Psi^1{}_{j,n_1,n_2}(x,y) \\ & + DS_{j+1}[n_1,n_2]\, \Psi^2{}_{j,n_1,n_2}(x,y) \\ & + DD_{j+1}[n_1,n_2]\, \Psi^3{}_{j,n_1,n_2}(x,y). \end{aligned} \quad (5)$$

Note that the term $SS_{j+1}[n_1,n_2]$ can be further decomposed recursively. The four 2-D DPWT coefficients $SS_{j+1}$, $SD_{j+1}$, $DS_{j+1}$, and $DD_{j+1}$ corresponding to the projection of $f(x,y)$ onto the subspaces $\bar{V}_j$, $\bar{W}_j^1$, $\bar{W}_j^2$, and $\bar{W}_j^3$, respectively. To derive the 2-D DPWT coefficients in a separable case, there exists a pyramid algorithm [2]. The algorithm can be represented in terms of matrix form. An example of $j=-3$ is shown as follows:

$$[SS_{-2}(n_1,n_2)] = \hat{H} \times [SS_{-3}(k_1,k_2)] \times \hat{H}^T, \quad (6)$$

$$[SD_{-2}(n_1,n_2)] = \hat{H} \times [SS_{-3}(k_1,k_2)] \times \hat{G}^T, \quad (7)$$

$$[DS_{-2}(n_1,n_2)] = \hat{G} \times [SS_{-3}(k_1,k_2)] \times \hat{H}^T, \quad (8)$$

$$[DD_{-2}(n_1,n_2)] = \hat{G} \times [SS_{-3}(k_1,k_2)] \times \hat{G}^T, \quad (9)$$

where $\hat{H}^T$ and $\hat{G}^T$ denote the transposes of $\hat{H}$ and $\hat{G}$, respectively. The filter matrices $\hat{H}$ and $\hat{G}$ are given by

$$\hat{H} = \begin{bmatrix} \hat{h}[0] & \hat{h}[1] & \hat{h}[2] & \hat{h}[3] & 0 & 0 & 0 & 0 \\ 0 & 0 & \hat{h}[0] & \hat{h}[1] & \hat{h}[2] & \hat{h}[3] & 0 & 0 \\ 0 & 0 & 0 & 0 & \hat{h}[0] & \hat{h}[1] & \hat{h}[2] & \hat{h}[3] \\ \hat{h}[2] & \hat{h}[3] & 0 & 0 & 0 & 0 & \hat{h}[0] & \hat{h}[1] \end{bmatrix} \quad (10)$$

and

$$\hat{G} = \begin{bmatrix} \hat{h}[1]-\hat{h}[0] & 0 & 0 & 0 & 0 & \hat{h}[3]-\hat{h}[2] \\ \hat{h}[3]-\hat{h}[2] & \hat{h}[1]-\hat{h}[0] & 0 & 0 & 0 & 0 \\ 0 & 0 & \hat{h}[3]-\hat{h}[2] & \hat{h}[1]-\hat{h}[0] & 0 & 0 \\ 0 & 0 & 0 & 0 & \hat{h}[3]-\hat{h}[2] & \hat{h}[1]-\hat{h}[0] \end{bmatrix}. \quad (11)$$

Eqs. (6)-(9) called the 2-D DPWT show a recursive decomposition process. It can be easily shown that the 2-D DPWT provides adequate octave components for perfect reconstruction. For an image decomposed into six stages, The reconstructed image by the inverse 2-D DPWT is shown in Fig.2.

### 2.2. The Operator Correlation Algorithm

Comparing the two matrices $\hat{H}$ and $\hat{G}$, it is obvious that the low pass filter has two points of time lag relating to the high pass filter at beginning process. This will cause a problem in the VLSI architecture design. To eliminate this time lag problem, the orthogonal property of even cyclic shift in the high pass filter can be used. That is,

$$\begin{aligned} & <\tilde{g}[n], \tilde{g}[(n+2m)_N]> = <\tilde{g}[u], \tilde{g}[u]\exp[j4\pi mu/N]> \\ & = \sum_{u=0}^{N-1} |\tilde{g}[u]|^2 \exp[-j4\pi mu/N] = 0, \end{aligned} \quad (12)$$

where $m \in Z$, $N=2^{-j}$, and $\tilde{g}[u]$ denotes the discrete Fourier transform of $\tilde{g}[n]$. By Eq.(12), one takes right circular shifting of $d-2$ elements in the $\hat{G}$ matrix, where $d$ denotes the discrete-time filter length. Then the modified matrix $\hat{G}_m$ can be yielded as

$$\hat{G}_m = \begin{bmatrix} \hat{h}[3]-\hat{h}[2] & \hat{h}[1]-\hat{h}[0] & 0 & 0 & 0 & 0 \\ 0 & 0 & \hat{h}[3]-\hat{h}[2] & \hat{h}[1]-\hat{h}[0] & 0 & 0 \\ 0 & 0 & 0 & 0 & \hat{h}[3]-\hat{h}[2] & \hat{h}[1]-\hat{h}[0] \\ \hat{h}[1]-\hat{h}[0] & 0 & 0 & 0 & 0 & \hat{h}[3]-\hat{h}[2] \end{bmatrix}. \quad (13)$$

Comparing Eq.(11) with Eq.(13), it can be found that the two vector spaces spanned by the four orthonormal row vectors in $\hat{G}$ and $\hat{G}_m$ are identical. However, employing the $\hat{G}_m$ and $\hat{H}$ in the 2-D DPWT, all the four band components can be computed synchronously and require same boundary data. Besides, for a filter with length $d$, the separate computation requires $d^2+d$ multiplications to compute each 2-D DPWT coefficient.

The modified 2-D DPWT can be further simplified by applying the $m$-shift operator correlation process ($o_m$) defined as follows:

Definition 1. Let $f(x,y)$ denote a $N \times M$ digital image and $w(k,\ell)$ denote a $K \times L$ operator, where $0<K \le N$ and $0<L \le M$. The $m$-shift operator correlation processes of $f(x,y)$ and $w(k,\ell)$, i.e., $o_m$ is defined by

$$b(i,j) = w(k,\ell)\, o_m\, f(x,y) \equiv \sum_{\ell=0}^{L-1} \sum_{k=0}^{K-1} f((i\cdot m+k)_K, (j\cdot m+\ell)_L) \cdot w(k,\ell),$$

where $b(i,j)$ is a $(\text{int}(\frac{N-1}{m})+1) \times (\text{int}(\frac{M-1}{m})+1)$ digital image and int($x$) denotes the integral part of $x$. With $m=2$ in $o_m$, the 2-D DPWT process can be rewritten by

$$[SS_{-2}(n_1,n_2)] = W_{LL}\, o_2\, [SS_{-3}(k_1,k_2)]; \quad (14)$$

$$[SD_{-2}(n_1,n_2)] = W_{LH}\, o_2\, [SS_{-3}(k_1,k_2)]; \quad (15)$$

$$[DS_{-2}(n_1,n_2)] = W_{HL}\, o_2\, [SS_{-3}(k_1,k_2)]; \quad (16)$$

$$[DD_{-2}(n_1,n_2)] = W_{HH}\, o_2\, [SS_{-3}(k_1,k_2)], \quad (17)$$

where $W_{LL}$, $W_{LH}$, $W_{HL}$, and $W_{HH}$ are called the 2-D DPWT operators defined as follows:

$$W_{LL} = [h(i)\cdot h(j)]_{i,j \in Z_4}; \quad (18)$$

$$W_{LH} = [(-1)^{3-j} h(i) \cdot h(3-j)]_{i,j \in Z_4}; \quad (19)$$

$$W_{HL} = [(-1)^{3-i} h(3-i) \cdot h(j)]_{i,j \in Z_4}; \quad (20)$$

$$W_{HH} = [(-1)^{i+j} h(3-i) \cdot h(3-j)]_{i,j \in Z_4}. \quad (21)$$

In general, there are $d \times d$ elements in each 2-D DPWT operators for a filter with length $d$. The elements in the operators are called the 2-D DPWT filter coefficients. To compute a 2-D DPWT coefficient, the 2-D operator correlation algorithm needs $d^2$ multiplications.

### III. Performance Analyses of Finite Precision

For VLSI implementation of the 2-D DPWT process, it is desirable to convert the real number of 2-D filter coefficients to finite precision integer. In this section, three performance analyses of a finite precision 2-D DPWT process are presented. It shows that more accuracy result can be derived by directly using the 2-D filter coefficients than using two transforms of the 1-D DPWT. In other words, fewer bits for filter coefficients representation is required in the 2-D operator correlation algorithm.

Since the input data of digital image are integral numbers, e.g., 8-bits, one defines the 2-D filter coefficients in $p$ bits precision and the intermediate 2-D DPWT coefficients in $q$ bits precision, where $q > p+8$. For simplicity in our analyses, the 2-D filter coefficients are normalized such that the sum of the filter coefficients in LL band is equal to one and the sums in other bands are all equal to zero. To have $p$ bits precision, let $I_{max} = 2^{p-1}$, we multiply each 2-D filter coefficient by $I_{max}$ and round the result to the closest integer value. Then all the 2-D filter coefficients for even number of $p$ can be converted to the integral numbers located in the half open region $[-I_{max}, I_{max})$. For odd number of $p$, the converted 2-D filter coefficients will locate in the open region $(-I_{max}, I_{max})$. To keep $q$-bits precision in the 2-D DPWT process, one divides all the 2-D DPWT coefficients in LL band, i.e., $SS_{j+1}$ by $I_{max}$ for next stage decomposition. The exact $q$ value can be determined by the maximum 2-D DPWT coefficients in an analysis.

To analyze round-off error effect, a finite precision performance of 2-D filters is evaluated. All the real values of original 2-D filter coefficients are firstly converted to $p$ bits precision integer values. Then, one divides the integers by $I_{max}$ and reconstructs the real number form of 2-D filter coefficients. The reconstructed filter coefficients are evaluated with the original coefficients for each band. The root-mean-square value of signal-to-noise ratio (SNRrms) is used as the measurement parameter. Let $d$ denote the filter length. One accuracy measurement result of LL band 2-D filter is shown in Fig.3 in which the horizontal axis denotes the precision of $p$ bits, where $I_{max} = 2^{p-1}$. Four Daubechies' filters with $d$=4, 6, 8, and 10 are evaluated. For comparison with the conventional method that uses 1-D filter coefficients, one first multiplies the 1-D filter coefficients ($h(n)$) by $\sqrt{I_{max}}$ and rounds to the closest integer value. Then, one constructs the integer representation of 2-D filter coefficients. Finally, one converts the integral 2-D filter coefficients to real values. By the same measurement method, the finite precision performance of the LL band 2-D filter is shown in Fig.4. In comparison with Fig.3 and Fig.4, it clearly reveals that the 2-D DPWT with the 2-D operator correlation algorithm can obtain better finite precision value of 2-D filter coefficients than with the conventional separate method that 1-D coefficients are used in both row and column transforms.

To analyze the finite precision performance of 2-D DPWT process, it usually uses practical signals and requires two accuracy measurements of the 2-D DPWT coefficients and the reconstructed signals. In our analyses, four images (baboon, lake, Lena, and peppers images) have been evaluated and four Daubechies' filters with $d$=4, 6, 8,and 10 are used. An image is recursively decomposed into six stages, where each subband image in the last stage has $8 \times 8$ dimensions. All the integral 2-D DPWT coefficients in each subband image of each stage are then converted to real value for accuracy measurement. The corresponding references in the comparison are derived by double precision real value. Choose the baboon image and let 2-D DPWT coefficients in all decomposition stages be 21-bits precision (i.e., $p$=12 and $q$=21), an accuracy measurement of finite precision 2-D DPWT coefficients is illustrated in Table 1. In the analyses of four images, the maximum 2-D DPWT coefficient is 534728 happened in the third stage of lake image with $d$=10 and $I_{max}$=2048. Since we are only interested in the 2-D DPWT process, the finite precision effect of inverse process is neglected. Hence, the converted real values of 2-D DPWT coefficients are directly used in the inverse 2-D DPWT process to derive the reconstructed image. Fig.5 shows the accuracy measurements of the reconstructed baboon images.

### IV. The Non-Separate VLSI Architecture

In the operator correlation algorithm, the four 2-D DPWT operators are parallelly performed by double shifting in both row and column orientations. Among the four operators, there exist reflection properties and high repetition of the 2-D filter coefficients. Based on the analysis of the operator correlation algorithm, a new VLSI architecture called non-separate architecture for the 2-D DPWT implementation is presented in this paper. The architecture requires interleaved input data that is similar in the data format to Vishwanath' architecture [17].

In examining the four 2-D DPWT operators, where the negative sign is neglected, it can be found that there exist two mirror reflections among the four 2-D DPWT operators.

The 2-D filter coefficients in $W_{LL}$ and $W_{LH}$ (or $W_{HL}$ and $W_{HH}$) have left-and-right mirror-image correspondence while those in $W_{LL}$ and $W_{HL}$ (or $W_{LH}$ and $W_{HH}$) have up-and-down mirror-image correspondence. The four operators will be synchronously used to process the same input data. To combine the four operator correlation processes into one processing manner, one can firstly multiply all the input data by their exact corresponding 2-D filter coefficients in $W_{LL}$ to generate the weighted input data. Then the LL band 2-D DPWT coefficients, i.e., $SS$ can be obtained by two data accumulation processes. For matching to input data format generally defined by row scanner, the data accumulation processes are consisted of one row accumulation followed by one column accumulation. In row accumulation, the weighted input data will be accumulated from left to right to compute the sum of $d$ length weighted data. In column accumulation, the row sums will be accumulated from top to bottom to obtain the coefficients $SS$. To obtain the coefficients $SD$, the row accumulation should be performed in opposite direction. By the similar way, one can obtain the coefficients $DS$ and $DD$ by changing the direction of column accumulation. Hence, in terms of the reflection properties, The 2-D operator correlation algorithm can be carried into the simple execution procedures described as: 1) Multiply input datum by 2-D filter coefficients to derive the weighted data. 2) Accumulate the weighted data in row orientation to compute the row sums. 3) Finally, accumulate the row sums in column orientation to derive octave data.

Based on the execution procedures, the non-separate architecture depicted in Fig. 6 is essentially consisted of three functional units, i.e., the parallel multipliers, the data accumulators, and the input data controller. The overall aspect of the proposed architecture is in the nature of a parallel processing structure in which the processing of each data accumulator is independent. Hence simple control timing is requested. System clock with frequency $f_S$ is employed in the input data controller and the clock timing with frequency $f_S/2^k$ is employed in the data accumulator in the $k$-th decomposition stage. The latency of 2-D DPWT coefficients is one system clock cycle. Since a system clock cycle will involve only one multiplication, two adds, a $p-1$ bits shifting, and data transmission delay. Hence, the proposed architecture will have shorter latency than the conventional separate architecture that needs at least two multiplies. For simplicity, one defines the original data sequence as $SS_J$ (●) and the intermediate LL band 2-D DPWT coefficients sequences as $SS_{J+1}$ (■), $SS_{J+2}$ (★), and $SS_{J+3}$ ( ▼ ) for the first, second, and third decomposition stages, respectively.

The parallel-multipliers architecture illustrated in Fig. 7 is to generate all the weighted input data. For the case of 1-D filter with length 4, there are ten different 2-D filter coefficients required in the 2-D DPWT process. Generally, for a 1-D filter with length $d$, the parallel-multipliers unit needs $d(d+1)/2$ multipliers.

All the data accumulators in Fig.6 are identical. One data accumulator can be used to derive the octave band components in one decomposition stage. Thus one can choose n data accumulators for n stages need. For a 1-D filter with length $d$, the data accumulator is consisted of $d$ row accumulators and one column accumulator. For an example with $d$=4, the detailed architecture of row accumulator is depicted in Fig.8 in which the block circumscribed by dash-line denotes the architecture for column boundary data handling. The architecture is essentially in the nature of a linear systolic array in which each cell contains only one adder (or one subtracter) and one register. To deal with the boundary data in two bands, two storage cells are requested to save the intermediate data. In general, for the case $d>4$, each band needs one de-multiplex and $(d-2)/2$ storage cells for saving the intermediate boundary data. The general case will be detailedly discussed in the next section.

To accumulate the row sums, the architecture of column accumulator is illustrated in Fig. 9. Essentially, the column accumulator is similar in architecture to the row accumulator except that the register in each cell is replaced by a shift registers buffer. The registers buffer is to transfer the row data format into column data format. In the column accumulator, the LL and LH bands components are accumulated downward while the HL and HH bands are in opposite direction. To save the intermediate row boundary data, a column accumulator also needs two multiplexes and two extra registers buffers depicted in Fig. 9. The multiplex makes the row boundary data be cyclically shifted in the registers buffer for (N-2) row scanning delay, where N denotes an image size. One major idea of the column accumulator design is to make the octave components in the last two rows be generated simultaneously. However, for next stage decomposition, the last row will be delayed by a row scanning time. The length of the registers buffers will be decreased by power of two as the decomposition stage increases. Since the registers buffers contain only replicated register cells, they can be considered identical in architecture.

The basic function of the input data controller depicted in Fig.10 is a shift registers buffer in which several switches are inserted. The goal of the switches is to intersperse several LL bands components into the original data sequence for next stage decomposition. The operations of a switch and its corresponding data accumulator are synchronous. In addition, the proposed architecture requests a simple control unit to generate the desired timing.

In a Verilog behavioral model simulation for the architecture verification, a three-stage decomposition process of $16\times16$ sequential images is taken as an example. In this simulation, the filter length $d$=4 is

assumed. To illustrate the simulation result, let symbols ●, ■, ★, and ▼ denote the data sequence of $SS_J$, $SS_{J+1}$, $SS_{J+2}$, and $SS_{J+3}$, respectively. Also, let symbols □, ☆, and ▽ denote the intermediate row boundary data of $SS_{J+1}$, $SS_{J+2}$, and $SS_{J+3}$, respectively. Since the octave bands components are derived simultaneously. Only the LL bands components are shown. The simulation result shows that the last row data of resolution level $J+1$ will be obtained during the first row in next frame image. The last row data of resolution level $J+2$ will be obtained during the second row in next frame image and so forth.

## V. Discussions and Conclusion

A 2-D operator correlation algorithm for performing the 2-D DPWT has been presented. The algorithm has merits of synchronous boundary data handling, low round-off error, and fast computation. Based on the 2-D operator correlation algorithm, a novel approach of non-separate VLSI architecture design has been proposed, too. The architecture is a parallel-like structure and has the features of short-time latency, short bit length request, and fast to derive intact octave band components for the purpose of perfect reconstruction. Due to high modularity and processing independence, the architecture is well suited for VLSI implementation. A Verilog behavioral model simulation for the architecture of 1-D filter length $d$=4 has been taken. For the general case of 1-D filter with $d > 4$, one needs more complex circuit to deal with the boundary data. A verified architecture of $d$=8 is illustrated in Fig.11 for column boundary data handling in a row accumulator. Since the column and row accumulators are identical in architecture. The architecture shown in Fig.11 can be easily expanded for row boundary data handling in column accumulators.

In time domain method for 2-D DPWT implementation, the VLSI architecture design usually needs to deal with a compromise among speed, complexity, filter length, decomposition stages, and hardware utility. Parallel processing can provide fast computation and simple architecture for data flow control. However, the hardware utility of parallel architecture will be decreased due to increasing either the filter length or decomposition stages. Because the produced DPWT coefficients in a DPWT decomposition process are decreased in power of two speed, the architecture requests low frequency clock to accumulate the data in low-resolution level. As a sequence, the hardware utility of overall system will be decreased while the decomposition stages are increased. Besides, for both row and column boundary data processing, Fig. 11 clearly reveals that almost same size of extra circuit and more complex controller are needed. Since the intermediate boundary data should be saved for a very long time, it also results in hardware utility decreasing. However, if only one stage is concerned and the boundary data handling is neglected, the proposed architecture has high hardware utility.

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Fig. 1. Result of imperfect reconstruction. (The boundary data are dropped).

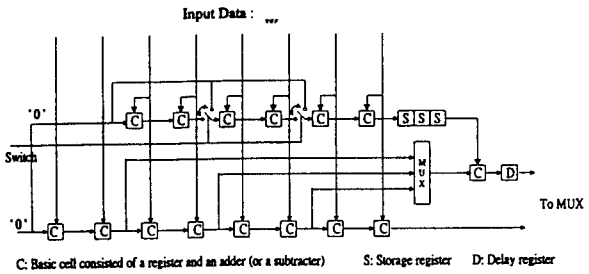


Fig. 11. Architecture of column boundary data handling for 1-D filter length $d$ =8.

Fig. 2. Result of perfect reconstruction.

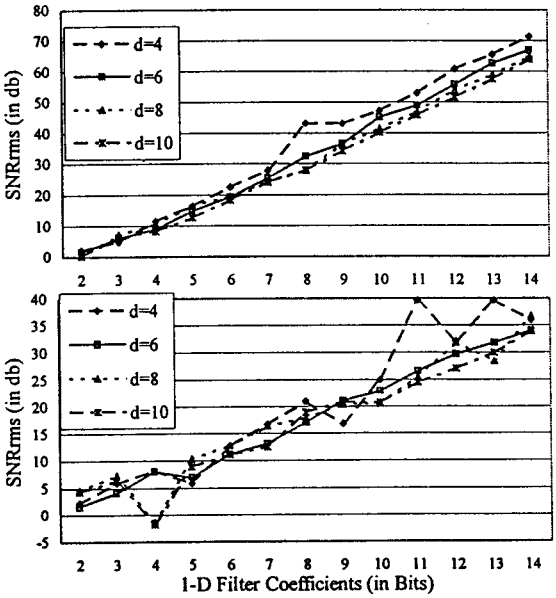


Fig. 3. Accuracy of the 2-D filter coefficients derived from 2-D operators.

Fig. 4. Accuracy of the 2-D filter coefficients derived from 1-D coefficients.

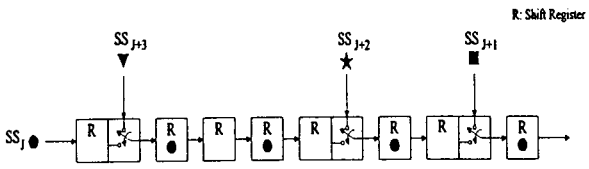


Fig. 10. Architecture of the input data controller.

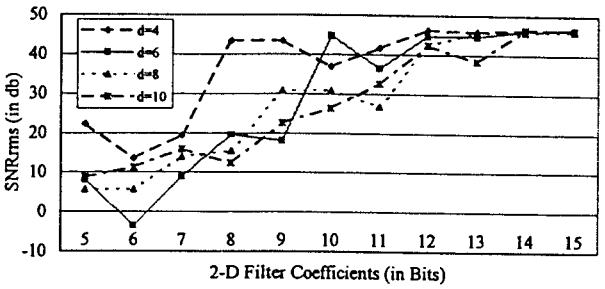


Fig. 5. Accuracy of finite precision 2-D DPWT process for reconstructed baboon image.

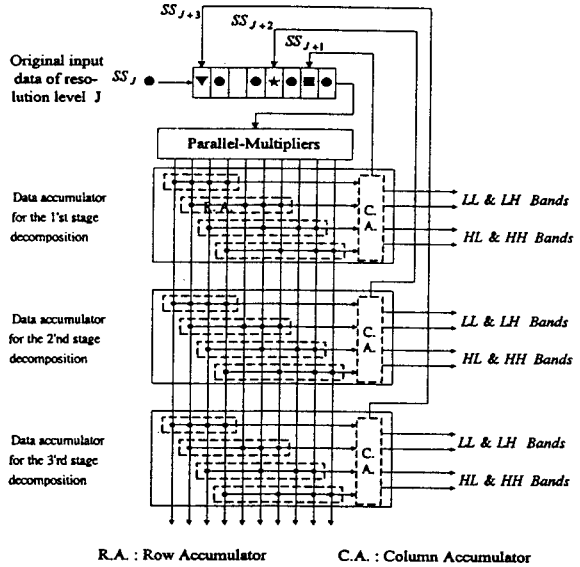


Fig. 6. The whole non-separate VLSI architecture for the 2-D DPWT implementation.

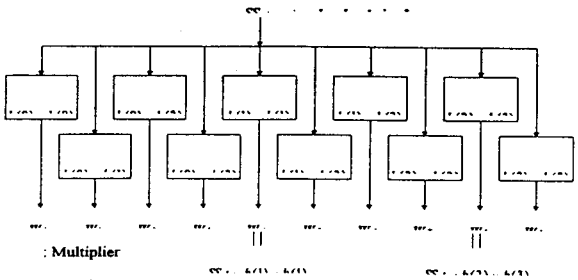


Fig. 7 Architecture of parallel-multipliers.

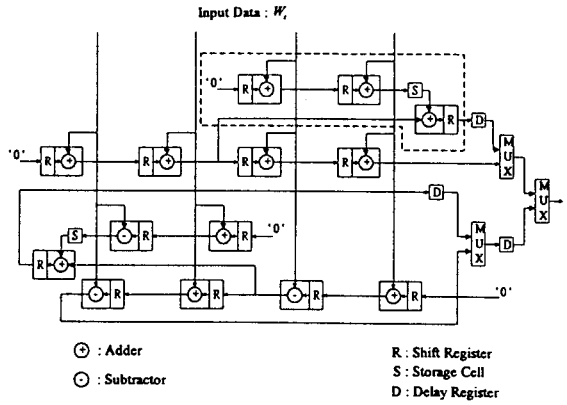


Fig. 8. Architecture of row accumulator.

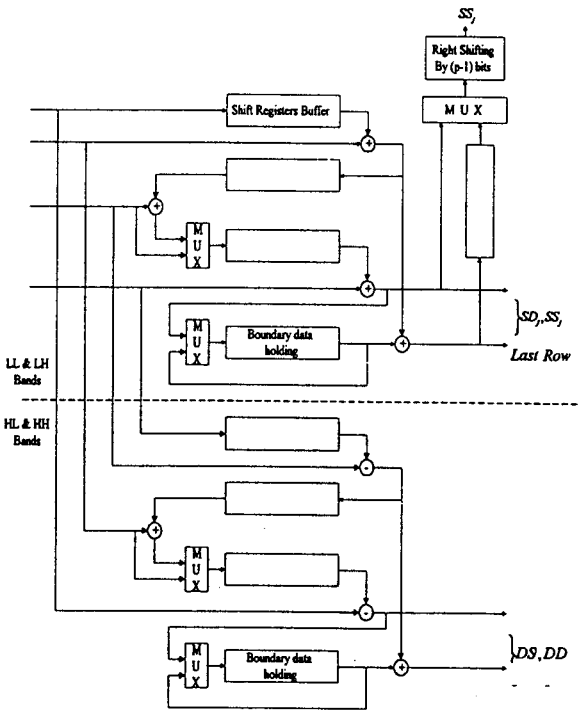


Fig. 9. Architecture of column accumulator.

Table 1. Accuracy of finite precision 2-D DPWT coefficients in baboon image (in db).

| *d* | Band | 1'st Stage | 2'nd Stage | 3'rd Stage | 5-th Stage | Last Stage | LL Band |
|---|---|---|---|---|---|---|---|
| 4 | LH | 86.28 | 81.67 | 76.30 | 80.26 | 138.82 | 133.07 |
| | HL | 74.84 | 77.45 | 75.52 | 87.02 | 138.81 | |
| | HH | 63.05 | 61.26 | 67.39 | 76.76 | 139.69 | |
| 6 | LH | 81.16 | 73.06 | 73.19 | 74.32 | 81.05 | 132.26 |
| | HL | 72.37 | 73.38 | 71.94 | 81.25 | 91.36 | |
| | HH | 62.50 | 63.53 | 66.59 | 76.41 | 111.46 | |
| 8 | LH | 84.67 | 77.63 | 77.73 | 79.91 | 113.64 | 103.43 |
| | HL | 75.63 | 73.71 | 75.08 | 86.82 | 126.74 | |
| | HH | 60.78 | 59.85 | 63.13 | 70.48 | 74.93 | |
| 10 | LH | 79.90 | 71.07 | 69.03 | 69.52 | 72.23 | 116.53 |
| | HL | 62.57 | 66.71 | 65.34 | 76.38 | 83.52 | |
| | HH | 61.85 | 61.17 | 66.20 | 74.21 | 86.57 | |