UNIVERSAL CURRENT INTEGRATION MODULE IC DESIGN FOR SMART BATTERY MANAGEMENT OF MOBILE HANDSETS†

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ABSTRACT

An efficient capacity estimator for batteries is the core of the success of the battery management. In this paper, we propose a general capacity measurement module for the current computation in the process of battery charging and discharging. Such a module can be included in a variety of battery management systems (or ICs). The simulation and testing results of the final chip prove the correctness of the design.

1. INTRODUCTION

Users of battery operated equipments, e.g., handset and notebook, often deem the battery as an unpredictable source of power. However, it is the only power source of the portable systems after all. The users always hope that the systems can remind them before the battery runs out. Thus, a smart battery manager is required in these portable systems. There are two major directions of improvements to battery management [4] :

1). giving the user a clear understanding of the battery's present capacity

2). enabling effective power management systems that take advantage of accurate information supplied by the battery to extend operating time.

A common and traditional battery management is to signal an alarm either to a display or to a speaker when the voltage of battery is below certain predefined level such that the user can replace the old battery with a new one. However, the smart battery manager should be able to achieve the following tasks besides the mentioned alarming function :

1). Alarms — battery about to run out

2). Control/Status/Error — the operating mode or the sleep mode

3). Predictive functions — how long will the battery supply at present status

4). Measured data — how much current is it supplying?

5). Battery characteristics — design capacity, cell chemistry, manufacturer's name and serial number

Although there have been a few battery manager IC available on the shelf, [1], [2], [9], most of them are not dedicated for wireless handsets. Power minder IC [1] can not detect over-current discharging, and needs extra circuitry to handle audio or video alarming. Gas Gauge IC [2] is pretty accurate regarding current measure, but the protocol is complicated and an extra EEPROM might be required. Battery protection IC [9] has not internal counter or RAM to process the required aforementioned smart battery functions.

Notably, owing to a fact that different batteries has their own I-V characteristics basing upon different type of the chemical material, e.g., NiH or Li, or manufacturing companies, the originally stored charge capacity routines might not function correctly if the battery is changed to another brand or type. Besides the current integration computation, other parameters are mostly dependent upon the battery brands and chemical materials, e.g., self-discharging, voltage depression, memory effect, etc. Hence, we tend to propose a general capacity measurement module for the current computation. Such a module can be included in a variety of battery management systems (or ICs).

2. CHIP DESIGN OF THE CURRENT INTEGRATION MODULE (CIM)

2.1. Computation of Battery Capacity by Current Integration

Let's use the NiH battery as an illustrative example to describe the whole scenario. The chemical reaction functions for a NiH battery in a charging cycle are as follows.

$$NiOOH + H_2O + e^- \rightarrow Ni(OH)_2 + OH^-$$

$$MH + OH^- \rightarrow M + H_2O + e^-$$

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reactions of a battery can be classified as either a electron-generating function or a reversible electron-absorbing function. If the same amount of the current (electrons) can be restored as that of the current dissipated in any earlier operations by a sophisticated re-charging scheme, the capacity of the battery can be restored. Hence, the battery capacity can be measured by a constant current (mA) times the amount of time (hours) which the constant current can be steadily maintained.

$$\text{battery capacity (mAH)} = I \text{ (mAH)} \times t \text{ (H, hours)}$$

where I denotes the constant current, and t is the duration that the current is provided.

2.2. Measurement of Current Integration

A simple idea to measure the total amount of current is by measuring the variation of the voltage on a pre-determined fixed resistor though a given time span. Then, the current integration can be computed by the voltage integration as the following equation.

$$\text{battery capacity (mAH)} = \int_{t_0}^{t} i(t)dt + C = \int_{t_0}^{t} \frac{v(t)}{r} + C$$

where C is a constant, $i(t)$ and $v(t)$ are the current and voltage though the resistor r in the time span from t_0 to t. Thus, the current integration is feasible.

Another factor to be noted is the time unit besides the voltage measurement. The system clock is used as the time unit to sample the voltage at r. Then, the sampled voltage is accumulated to be the total voltage amount, which is stored in a long accumulation register. The accumulation register (called accumulator) should possess the processing capability of carry (plus) and borrow (minus) bits for charging and discharging operations, respectively.

2.3. Usage of Current Integration Module (CIM)

Since the CIM is designed for applications in mobile handsets, we have to address the spatial relationship of the baseband microprocessor (i.e., host control unit), the battery pack, and the CIM in the discharging and the re-charging mode, respectively. Referring to Fig. 1, a simplified battery control system inside of a mobile handset is shown. When the handset is used in operation, regardless of idleness or transmitting, the VR2 of the CIM is connected to the negative polarity of the battery. The voltage difference of VR2 and VR is converted into digital signals by an ADC (analog-digital converter). Thus, the current integration function of CIM is proceeded such the remaining charge capacity of the battery can be calculated.

As for the re-charging operation of the battery, Fig.2 reveals the details. VR2 is connected to the negative polarity of the charging device. Thus, the voltage tal signals for the following integration and computation of the capacity of the battery.

2.4. Schematic Design of CIM

Note that the maximal idle time of currently commercial handsets is around 225 hours. $225 \times 60 \times 60 \times 10^6 = 8.1 \times 10^{11}$ μs. Hence, we use a total of 2^{29} timing units to record the current integration values is much more than needed. Besides, note that the discharging current of the handset in working is in the range of $140 \sim 550$ mA, while the idle current is in the range of $5 \sim 45$ mA. Since there is a pretty large difference between these currents, we select the "working" current as the calibration of measurement of the current. As for the idling current, it is adjusted with self-discharging current.

Referring to Fig. 3, the description of the internal circuits of CIM is given as follows.

A. The input voltage, VR, is fed through the external resistor, r. Meanwhile, a number of 8 reference voltages denoted by VOT0-VOT7 are produced by a resistor voltage-dividing network called "reference voltage generator" (RVG), as shown in Fig. 4. The reference maximal and minimal voltage of the resistor voltage-dividing network is fed externally by VR1 and VR2, respectively. The range between VR1 and VR2 is equally divided into 250 levels. The lowest eight levels, i.e., 1/250 to 8/250, of the voltages are generated by the "reference voltage generator" module, and used as reference voltages. The VR is then compared with the reference voltages in the "voltage comparator" (VC) module, as shown in Fig. 5, such that the measured analog VR can be converted into a digital signal.

B. The output digital signal of the "voltage comparator" module is re-encoded into a one-hot encoding format in the "one-hot encoding circuit" (OHE) module for following processes. The detailed circuit of the "one-hot encoding circuit" is given in Fig. 6.

C. The results of the "one-hot encoding circuit" is thus decoded into a binary representation by the "one-hot to binary code conversion circuit" (OH2B) module in Fig. 7 for the convenience of further processing.

D. The core of the integration operation is composed of a two cascaded DFFs and a 3-bit adder. The addition is executed at every clock cycle such that the integration is achieved. If there is any carry occurred, the clock of the next stage, i.e., the counter, will be triggered. That is, the integration of the current is recorded. An example is given to illustrate the operation of the above mentioned modules. Assume the VR is set to 0.07 V while the VR1 = 5.0 V and VR2 = 0.0 V. Table 1 shows the results of each of the mentioned modules.

E. If the input voltage, VR, is not located in the predefined range, "voltage bound checker circuit" (VBC) is in charge of monitoring such a scenario. The output, "OVERVOLTbar" = 0, indicates that VR is smaller

"UNDERVOLT" = high, represents that VR is higher than the upper bound. The circuit is shown in Fig. 8.

F. If the user tends to modify or preset the integration value, a total of 32 bits of data are divided into 4 bytes which are sequentially selected by "DCRHDIEN" and "DCRLDIEN" signals. These 4 bytes are fed into the 3 bits of "3-b FA" and the combination of 29 bits of "13-b counter" and "16-b counter" in Fig. 3.

G. In the interface with the control uP host, the mentioned 32 bits are again divided into 4 bytes, which are respectively selected by "DCRHDOEN" and "DCRLDOEN," and delivered at "DATA0-DATA7" sequentially.

H. The total 32 bits to record the integration resulted are composed of a high 29 bits in the 2 counters and a low 3 bits in the full adder in Fig. 3. Assume the voltage (current) is sampled once per second. Thus, the 29 bits can record up to 2^{29} data which is far than enough.

2.5. Pin-out considerations

Although the proposed CIM design is for the battery management, its pin count is not supposed to be as restricted as the pin count of other battery management ICs. The reason is the CIM is deemed as a universal module which is capable of being integrated with other peripherals such as RAMs and uPs. The total pin count is 28. The physical pin-out of the proposed CIM chips is listed as follows.

A. Power Pins : Since the battery management is not a high-speed operation, there is no need to concern the switching noise coupled from DC power to AC power. Hence, we merge the DC power pair and AC power pair to be one power pair only in order to save some pin count.

B. Input and Output Pins : They are respectively described in Table 2 and Table 3.

2.6. Design Hierarchy

The entire chip is designed in the CADENCE environment along with UMC (United Microelectronics Co.) 2P2M 0.25 μm CMOS technology. The design hierarchy is shown in Fig. 9. The power supply is 5.0 volts.

3. HSPICE SIMULATION & REAL CHIP TESTING

3.1. Chip simulation and implementation

Simulation of Voltage Comparator : Since the comparison of the input VR signal and the reference voltages plays a key role in the entire design, we must make sure that the function of this analog part is correct. Referring to Fig. 10, the input VR waveform is shown in the top stripe, while the rest stripes are the converted results in of the design.

Post-layout Simulation : Post-layout simulation is a required verification step to sign off a chip to the foundry. Fig. 11 illustrates part of the post-layout simulation results, which is the output waveform of "voltage comparator" module. The result turns out to be correct.

The entire chip layout is given in Fig. 12. The maximal operating clock rate is 10 MHz which is far than needed in the battery management. The chip have been approved by CIC (Chip Implementation Center) of NSC (National Science Council). The chip number is U05-88C-06u.

Chip testing and measurement : HP 1660CP logic analyzer/pattern generator is used to test and measure the functionality and accuracy of the fabricated chip. Table 4 is the measured data of the ADC. Fig. 13 is the comparison of the theoretical and physical ADC conversion curves of the chip. Notably, the theoretical conversion result can be met by shifting the measured physical conversion result by one bit owing to that there is a nearly constant multiplication factor of 2. Fig. 14 and Fig. 15, respectively, reveals two measured examples of $V_{in} = 0.046, 0.073$, produced by HP 1660CP. The results are more than appealing. At last, Fig. 16 shows the die photo of the CIM chip.

4. CONCLUSION

We have proposed a universal and feasible design for a current integration component which can be used for developing battery monitor ICs and circuits. The design methodology of the CIM is practical and cost-efficient. The simulation results turn out to be very appealing. Besides, the measurement and testing results of the physically fabricated chip also verify our design.

5. REFERENCES

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RVG	VC	OHE	OH2B
0.02 V	0	0	
0.04 V	0	0	
0.06 V	0	1	
0.06 V	1	0	011
0.08 V	1	0	
0.10 V	1	0	
0.12 V	1	0	
0.14 V	1	0	
0.16 V	1	*	

Table 1 : An example of the signal conversion. ("*" denotes unknown.)

001	1	0.02	0.012
010	2	0.04	0.024
011	3	0.06	0.032
100	4	0.08	0.048
101	5	0.10	0.056
110	6	0.12	0.070
111	7	0.16	0.084

Table 4 : The ADC input voltage ranges.

Pin Name	Function
VR	The voltage on the external resistor is read by this pin.
VR2	In fact, it is the negative polarity of the battery pack, i.e., the minimal voltage.
PD0 - PD7	byte-wide data bus.
CIN	An enable signal for the host system to preset or modify the integration data.
CLK	A clock signal to trigger a current (voltage) accumulation.
DCRHDIEN, DCRLDIEN	Selection signals to select which byte is to be preset or modified. "00" for Bit0-Bit7 = PD0-PD7, "01" for Bit8-Bit15 = PD0-PD7, "10" for Bit16-Bit23 = PD0-PD7, and "11" for Bit14-Bit31 = PD0-PD7, respectively.
DCRHDOEN, DCRLDOEN	Selection signals to select which byte is to be output. "00" for DATA0-DATA7 = Bit0-Bit7, "01" for DATA0-DATA7 = Bit8-Bit15, "10" for DATA0-DATA7 = Bit16-Bit23, and "11" for DATA0-DATA7 = Bit14-Bit31, respectively.

Table 2 : The functions of input pins.

Pin Name	Function
DATA0 - DATA7	The byte-wide integration result data bus.
OVERVOLTbar	When "0", it indicates that the input VR is larger than the maximal voltage of the acceptable range.
UNDERVOLT	When "1", it shows that the input VR is lower than the minimal bound of the acceptable voltage range.

Table 3 : The functions of output pins.

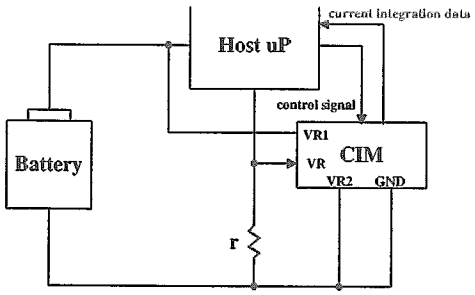

Figure 1: discharge scenario

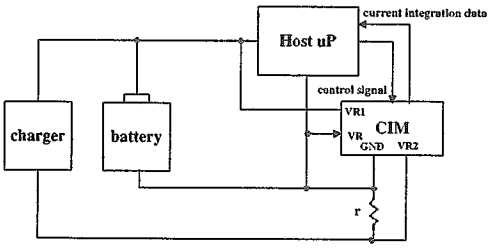

Figure 2: charging scenario

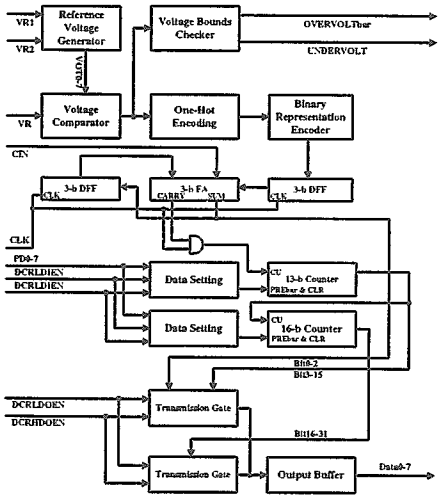

Figure 3: block diagram of CIM

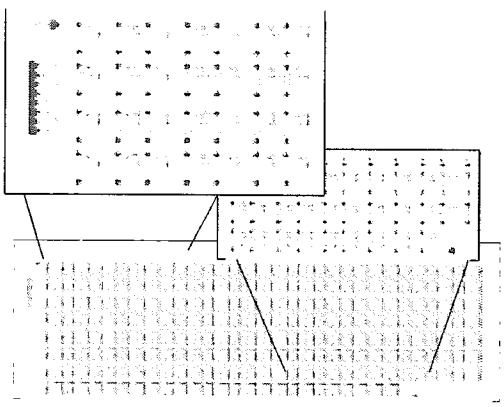

Figure 4: reference voltage generator

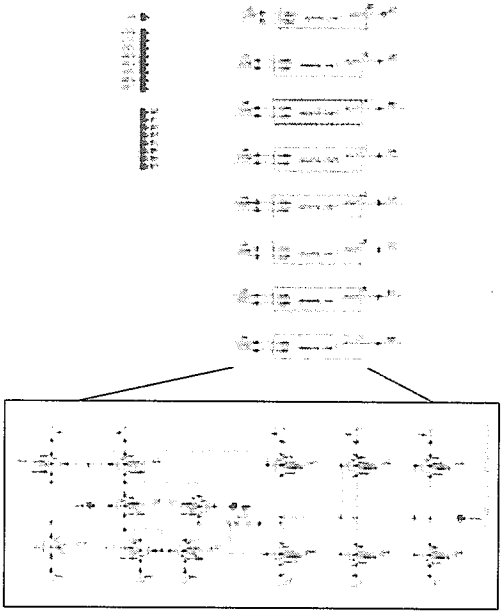

Figure 5: voltage comparator

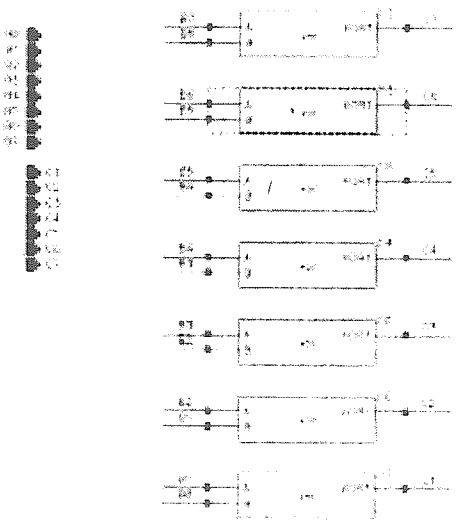

Figure 6: one-hot encoding circuit

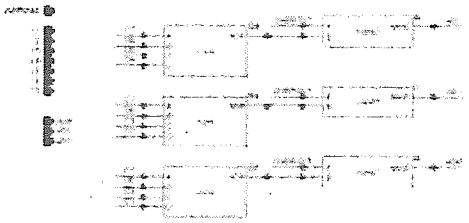

Figure 7: one-hot to binary code conversion circuit

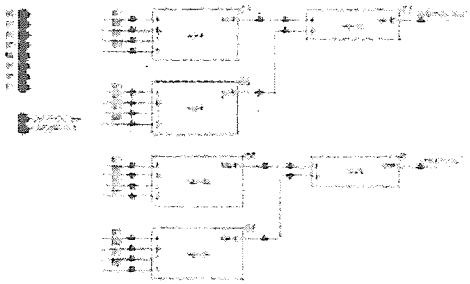

Figure 8: voltage bound checker circuit

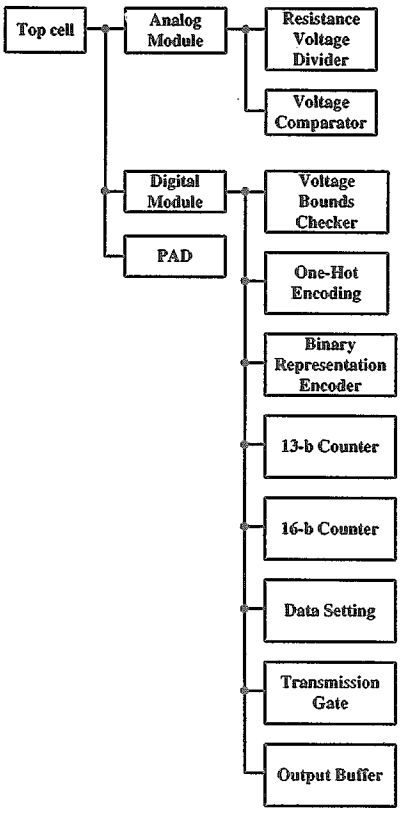

Figure 9: design hierarchy

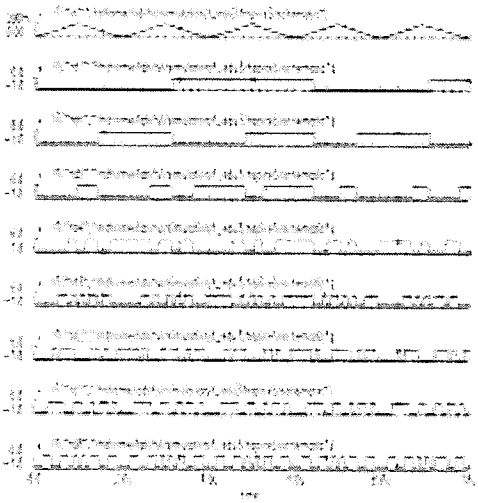

Figure 10: simulation results of the voltage comparator and the encoders(rd0-7=Bit0-7)

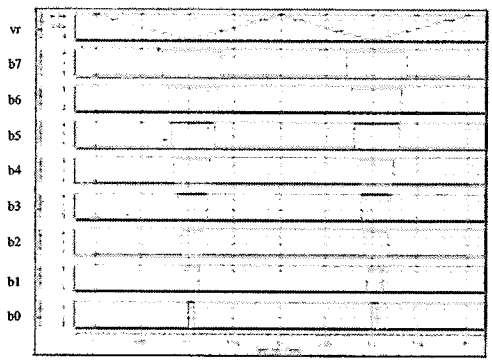

Figure 11: post-layout simulation waveforms

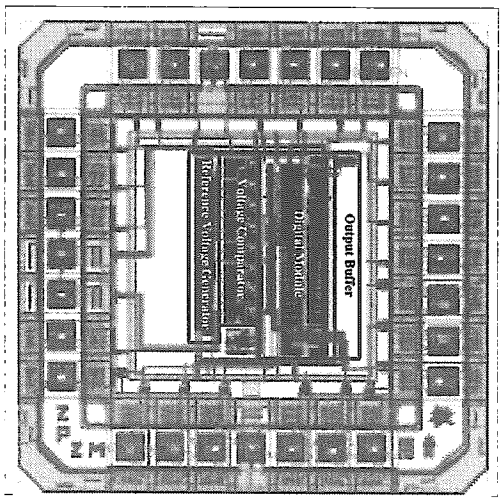

Figure 12: CIM chip layout

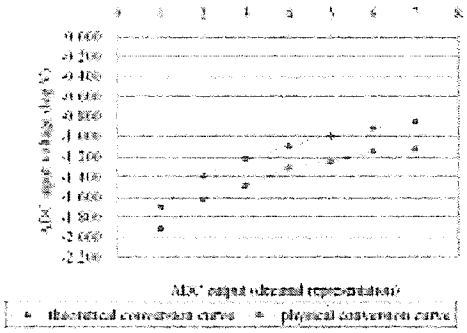

Figure 13: the comparison of the theoretical and physical ADC conversion curves of the chip

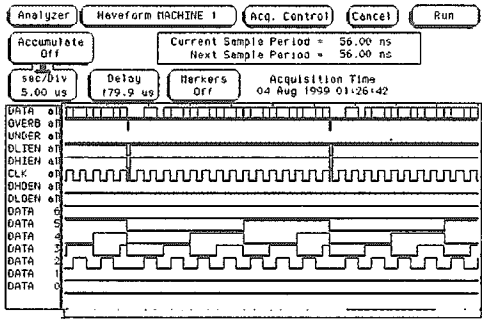

Figure 14: measured example of Vin = 0.046

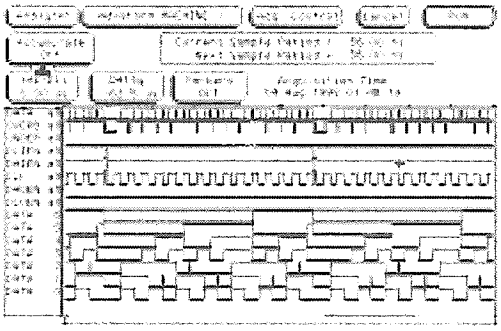

Figure 15: measured example of Vin = 0.073

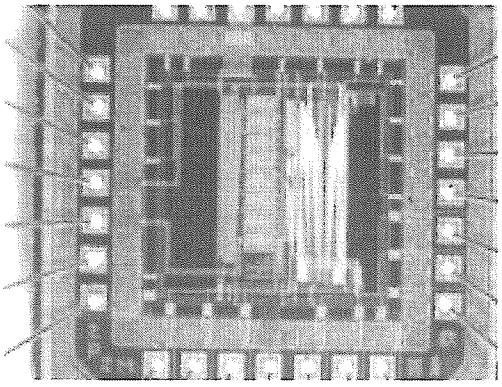

Figure 16: die photo of the CIM