A New Architecture of Rom-Less Quadrature Direct Digital Frequency Synthesizer

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Abstract

This paper presents the design of ROM-less quadrature Direct Digital Frequency Synthesizer (DDFS) by using trigonometric angle sum formula. The proposed DDFS consists of two adders and two multipliers to generate quadrature outputs. The results are simulated by using 0.35μm CMOS process technology. The spurious-free dynamic range (SFDR) is about 100dB, runs up to 100MHz and consumes 38.8mW at 3.3 V.

Index Terms — Direct Digital Frequency Synthesizer (DDFS), frequency synthesizer, ROM-less.

INTRODUCTION

In modern wireless communication systems, Direct Digital Frequency Synthesizer (DDFS) is adopted because of its good properties such as: fast frequency switching, fine frequency resolution, widely bandwidth, continuous phase frequency switching and good spectral purity.

A conventional ROM based DDFS, as shown in figure 1, usually consists of a phase accumulator, a ROM lookup table to generate sin and cosine function, a digital to analog converter (DAC), and a low-pass filter (LPF). In figure 1, f_{ctrl} decides the accumulator step in the phase accumulator and f_{clk} is the operation frequency of the DDFS. Assume the phase accumulator is M-bit. The output frequency of DDFS can be written as:

$$f_{out} = f_{ctrl} / 2^{M} \cdot f_{clk} \quad (1)$$

There are three main factors that determine the signal purity: 1) the phase quantization due to finite resolution of the phase accumulator; 2) amplitude quantization noise due to finite resolution of the DAC; and 3) static and dynamic nonidealities of the DAC [1]. The ROM size increases exponentially as the bit number of input increasing, and it will cause high power dissipation and occupied huge areas. In recent researches [2], many methods were proposed to solve these problems by compressing ROM size.

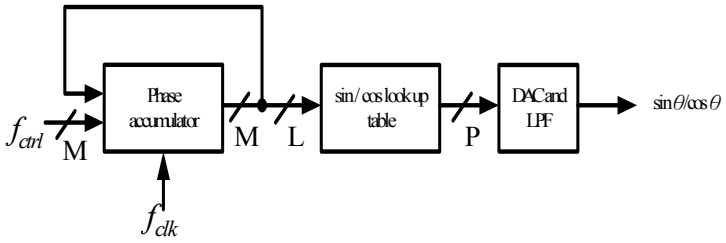

Figure 1 Conventional architecture of the ROM-based DDFS

ROM-less DDFS, as shown in figure 2, is another architecture to improve the drawbacks of the ROM-based DDFS in power and area. A lot of algorithms were proposed to implement this architecture, e.g. second-order parabolic approximation proposed by Sodagar et al. [3], polynomial interpolation technique proposed by Caro et al. [4], and CORDIC method proposed by Tahir et al. [5]. In the paper we propose a new algorithm and architecture to compute sine/cosine values by using trigonometric angle sum formula. The proposed architecture is implemented with 0.35μm CMOS cell-based library.

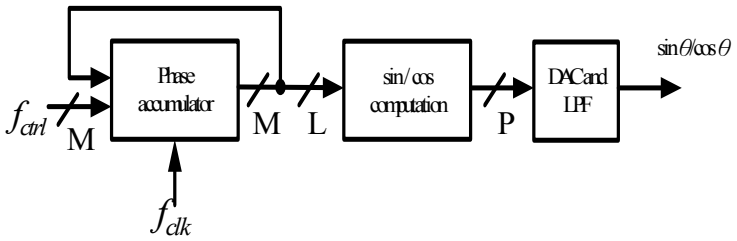

Figure 2 Conventional architecture of the ROM-less DDFS

PROPOSED DDFS ALGORITHEM

The quadrature output sequences of the proposed DDFS are as follows:

$$\sin\theta_1, \sin\theta_2, \sin\theta_3, \ldots, \sin\theta_n . \quad (2)$$
$$\cos\theta_1, \cos\theta_2, \cos\theta_3, \ldots, \cos\theta_n . \quad (3)$$

From equations (2) and (3), the difference of two successive sine/cosine values of outputs can be expressed as:

$$\Delta_{sin} = \sin\theta_{k+1} - \sin\theta_k \quad (4)$$
$$\Delta_{cos} = \cos\theta_{k+1} - \cos\theta_k , \quad (5)$$

where $\sin\theta_k$ and $\cos\theta_k$ are the k-th quadrature outputs of the DDFS, respectively. From equation (2) and (4), the value Δ_{sin} can be rewritten as equations (6):

$$\Delta_{sin} = \sin\theta_{k+1} - \sin\theta_k$$
$$= \sin(\theta_k + \theta) - \sin\theta_k, \quad (6)$$

where θ is the k-th increment phase angle.

According to the trigonometric angle sum formula, the equation (6) can be rewritten as:

$$\Delta_{sin} = \sin\theta_k \cdot \cos\theta + \cos\theta_k \cdot \sin\theta - \sin\theta_k$$
$$= \cos\theta_k \cdot \sin\theta + \sin\theta_k \cdot (\cos\theta - 1),$$
$$= \cos\theta_k \cdot (\theta - \theta^3/3! + \theta^5/5!...) + \sin\theta_k \cdot (-\theta^2/2! + \theta^4/4!...),$$
$$= \cos\theta_k \cdot \theta - [\sin\theta_k \cdot (\theta^2/2!..) + \cos\theta_k \cdot (\theta^3/3!..)] \quad (7)$$
$$= \cos\theta_k \cdot \theta - \delta$$

From equation (7) it supposes that each increment phase angle is small enough and δ can be dropped. Equation (7) can be rewritten as follow:

$$\Delta_{sin} = \cos(\theta_k) \cdot \theta - \delta,$$
$$\sin\theta_{k+1} - \sin\theta_k = \theta \cdot \cos\theta_k - \delta \quad (8)$$

Thus the sine value of DDFS can be written as equation (9):

$$\sin\theta_{k+1} = \sin\theta_k + \theta \cdot \cos\theta_k - \delta. \quad (9)$$

The cosine value of DDFS can be calculated in the same way as sine, and then the result is shown as equation (10).

$$\cos\theta_{k+1} = \cos\theta_k - \theta \cdot \sin\theta_k - \delta', \quad (10)$$

where δ' is $[\sin\theta_k \cdot (-\theta^3/3!..) + \cos\theta_k \cdot (\theta^2/2!..)]$. The equation (9) and (10) can be combined as:

$$\begin{bmatrix} \sin\theta_{k+1} \\ \cos\theta_{k+1} \end{bmatrix} = \begin{bmatrix} 1 & \theta \\ -\theta & 1 \end{bmatrix} \cdot \begin{bmatrix} \sin\theta_k \\ \cos\theta_k \end{bmatrix} + \begin{bmatrix} -\delta \\ -\delta' \end{bmatrix}. \quad (11)$$

In equation (11), control word θ is a variable value, and the initial values of sine and cosine are 0 and 1, respectively. Thus, by controlling the value of the θ, the output frequency of the DDFS can be tunable.

ARCHITECTURE OF THE PROPOSED DDFS

In this section, the architecture of DDFS based on the above algorithm will be presented. The architecture can be deduced from equation (11). Figure 3 shows the architecture of the proposed DDFS. In this architecture, the DDFS is only implemented by two adders and two multipliers.

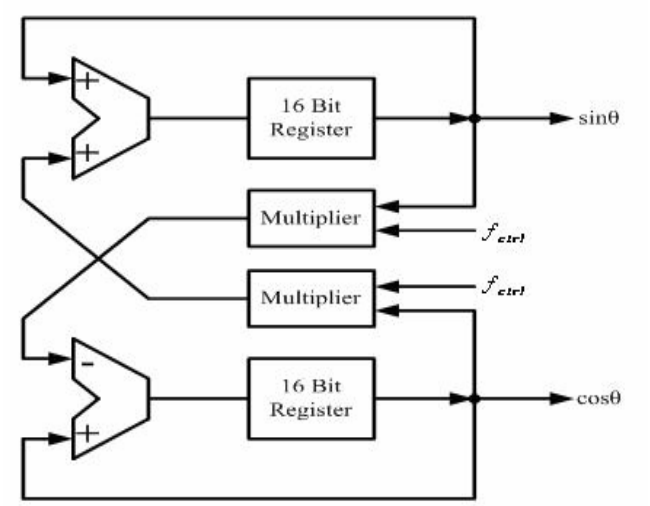

Figure 3 Architecture of the proposed ROM-less DDFS

SIMULATION AND RESULTS

The proposed DDFS is implemented by 0.35μm TSMC CMOS technology. It is operated at 3.3 V and f_{clk} is set at 100MHz. Figure 4 shows the waveform of sine/cosine with different FCW by Modelsim. Figure 5 shows the SFDR tendencies of the proposed DDFS.

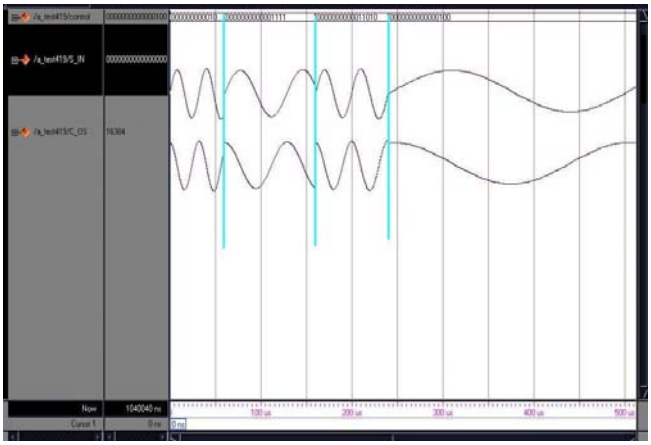

Figure 4 sine/cosine waveforms with different FCW simulated by ModelSim.

In measuring power consumption, 5,000 random patterns of FCW are generated feed into DDFS to simulate the average power. The SFDR of the proposed DDFS is about 100 dB. The power consumption is 38.8mW at 100MHz of Clock frequency. Figure 6 and Figure 7 show 105dB of SFDR in the simulation result and the difference between the ideal cosine function and the simulation results of proposed DDFS by using MATLAB. Figure 8 shows the difference error bounded by $6*10^{-3}$ between ideal cosine and the output of DDFS. The chip layout is depicted in figure 9. The chip area is about 1200 * 1200μm including pad and core. The gate

count is about 6186 calculated by the aid of Design Compiler. Table 1 and Table 2 shows the comparison of the properties with the other recently researches. The *Normalized Area*, the area normalized to a 1 *um* technology, is defined as follows:

$$Normalized\ Area = \frac{Area}{(Techno\log y/1um)^2}. \quad (12)$$

The *Power Efficiency* is defined as follows [6]:

$$Power\ Efficiency = \frac{Power}{Frequency}. \quad (13)$$

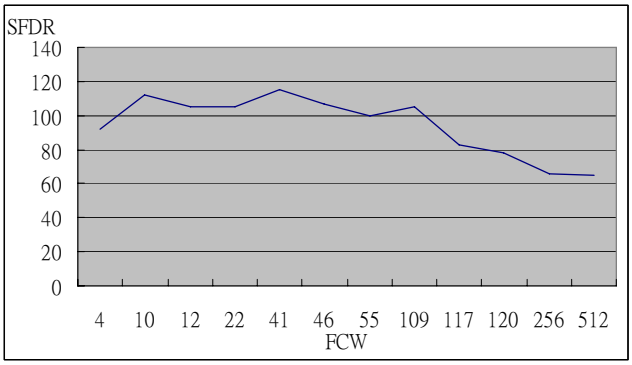

Figure 5 SFDR tendencies of the proposed DDFS

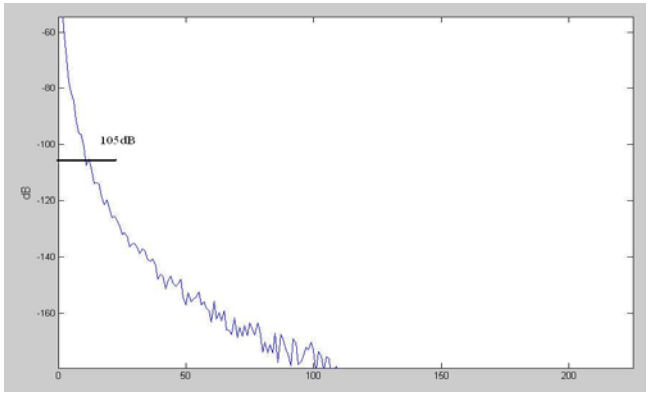

Figure 6 SFDR of the DDFS

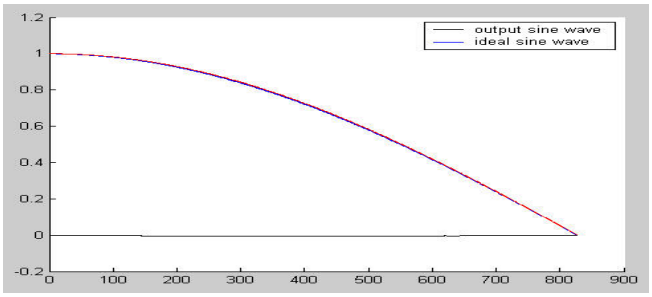

Figure 7 The difference between ideal cosine function and simulation results

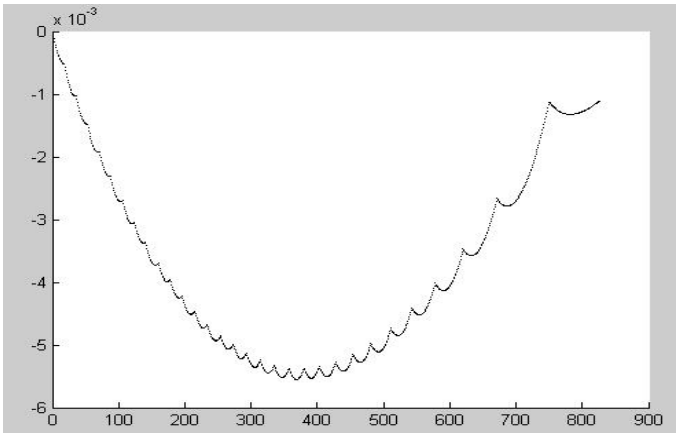

Figure 8 The error values between ideal cosine function and simulation results

Table 1 The comparison of the properties with the other recently researches.

	Ref.[6]	Ref.[7]	Ref.[8]	This work
Output word length	14 bits for sin/cos	14 bits for sin	10 bits for sin	16 bits for sin/cos
Process (μm)	0.25	0.5	FPGA	0.35
SFDR(dB)	100	91	64.2	100
Adders (bits)	three adders	four adder/sub	five adders	two 16 bit adders
Multiplier (bits)	two square circuits one mult.	Three 14*14 mult.	Two muls. (10*10 and 13*13)	Two 16*16 mult.

Table 2 The comparison of the properties with the other recently researches.

	Tech. process	Sin / Cos	SFDR (dB)	Output(bits)	Nor. Area (mm^2)	*Pe* (mW/MHz)
Ref. [9]	0.35	Yes	58	11	1.22	0.29
Ref. [10]	0.35	Yes	80	N/A	3.6	0.44
Ref. [11] Ref. [12]	0.35	No	84.6	13	2.53	0.13
This work1	0.35	Yes	100	16	4.33	0.38
This work2	0.18	Yes	100	16	N/A	0.04
Ref. [13]	0.18	No	70	12	1.23	0.034
Ref. [14]	0.18	Yes	84	13	2.78	0.5

CONCLUSIONS

In this paper, we present a ROM-less quadrature DDFS by using trigonometric angle sum formula and the definition of DDFS. It only requires two adders and two multipliers to calculate the sine/cosine function. The advantages of the proposed DDFS are low circuit complexity and occupying small chip area.

Acknowledgements

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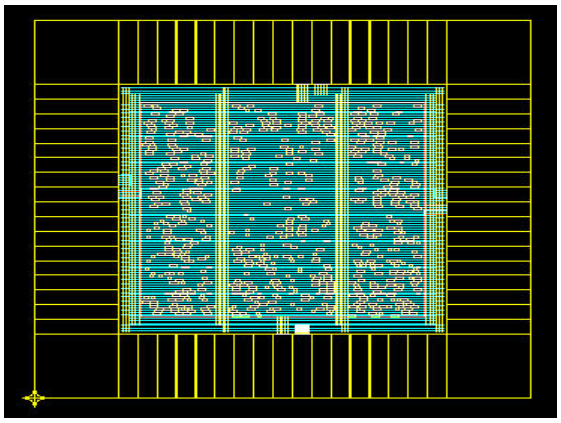

Figure 9 The chip layout of prototype IC

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