A Sweeping Mode CMOS Capacitive Fingerprint Sensor Chip

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ABSTRACT

In this paper, a sweeping mode capacitive sensor chip for fingerprint acquisition is presented. Based on capacitive fingerprint sensing, sweep capacitive sensor structure and readout circuit are proposed to grab the induced capacitance by the finger directly touched on the sensor plate. A test chip of 8×128 capacitive fingerprint sensor array is implemented in a standard 0.35-μm CMOS technology. Including the sensor array and peripheral digital control circuit, the chip area is 7307.1μm×748μm.

1: INTRODUCTION

Nowadays, the mobile applications like PDAs, notebook computers and cellular phones bring us convenient yet inimical threat of privacy. The more convenient these mobile applications are, the more significant the issue on personal security is. The demand of user authentication is becoming more and more important to protect against illegal access of personal mobile applications. Conventional protection schemes such as personal identification number (PIN) or password may be replaced by biometrics technologies. A lot of biometrics technologies have been developed for user authentication. For example, face, fingerprint, hand geometry, keystroke dynamics, hand vein, iris, retinal pattern, signature, voice print, facial thermogram, odor, DNA, gait, and ear recognition are different biometrics technologies that are either widely used or under investigation [1]. Many researchers make efforts on fingerprint authentication because of the properties of low-cost, reliability and technical soundness.

Up to the present, optical scan is the most common sensing type for fingerprint image acquisition. However, optical scan needs lens, light source, and some mechanical facility, which may provide the outstanding precision but hard to be embedded in mobile applications. In order to achieve the fingerprint acquisition on a single chip, we may prefer that devices can be totally realized by VLSI technology. A sensor integrated with readout circuit compatible of standard CMOS process may be more attractive. However, the sensor area which is needed for a complete fingerprint image is around above 1x1cm^2, so the cost of sensor chip is greatly increasing. Therefore, as shown in the Figure 1, making the chip be a log strip to much reduce the chip area and cost, pieces of fingerprint image can be sequentially grabbed just by sweeping finger over the chip. By software processing, a complete fingerprint image is available.

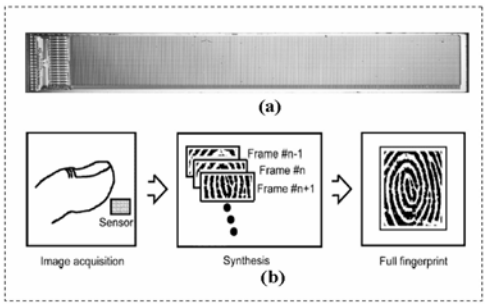


Fig. 1 Sweeping mode sensor array

Capacitive fingerprint sensors with the inexpensive and direct-touch properties have been proposed [2]–[6]. Our work in this paper reports a sweeping capacitive sensor structure and readout circuit based on capacitive sensing type fabricated by a standard CMOS process. Based on our previous work [7], a circuit design of sweeping mode capacitive fingerprint sensor chip is presented.

The paper describes a sweep capacitive sensing scheme that integrates both fingerprint sensor array and readout circuit on a single chip. The sensor is constructed by using top three metal layers of a standard 4-Metal CMOS process. The sensor readout is composed of a few switches and simplified control logic. The paper is organized as follows. First, the general principle of capacitive sensing for fingerprint is depicted in section 2. In section 3, the architecture of the proposed fingerprint sensor chip is described, along with the details of its circuit implementation. The experimental results are given in section 4. Finally, a conclusion is addressed in section 5.

2: PRINCIPLE OF FINGERPRINT ACQUISITION BY CAPACITIVE SENSING

Figure 2 shows the basic sensing operation of a capacitive fingerprint sensor. In microscopic scale, the surface of the fingerprint may have deeper part like a valley or more elevated part like a ridge. As the surface of the fingerprint approaching the sensor array, a few to some tenths fF of capacitance can be induced according

to the distance between the surface and the sensor plate. Intuitively, so called ridge part will produce a larger capacitance, C_{sr} ($C_{sr} = C_1 = \frac{\varepsilon_1 A}{d_1}$); while the valley part is responsible of a smaller capacitance, C_{sv} ($C_{sv} = C_1 | C_2 = \frac{1}{\frac{d_1}{\varepsilon_1 A} + \frac{d_2}{\varepsilon_2 A}}$). By recognizing these variations on capacitance value, the valley and ridge of fingerprint pattern can be constructed.

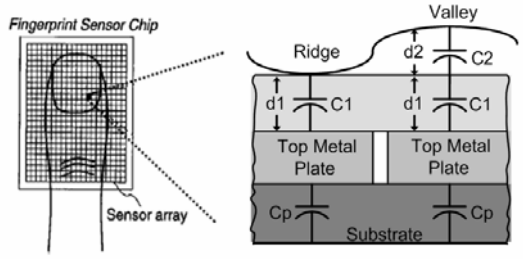


Fig. 2 Capacitive fingerprint sensing

The difficulties of capacitive sensing arise from the tiny change on the capacitance, especially more critical as the disturbance from the parasitic capacitance near the readout circuit. Through the efforts on improving the circuits, the capacitive sensing scheme can gain more benefits on performance, stability and reliability**.**

3: THE ARCHITECTURE AND IMPLEMENTATION OF PROPOSED CIRCUIT

Based on the previous design [7], we think about the practicability. Therefore, we proposed the sweep mode, and its type is 8 x 128 sensor array structure. We show the whole architecture of 8 x 128 sensor array in Figure 3. When a frame is scanned over, the end of frame signal will be generated by the last row and column select signals. A simple 4-bit flash A/D converter is also included to transform the sensed analog signal into digital codes.

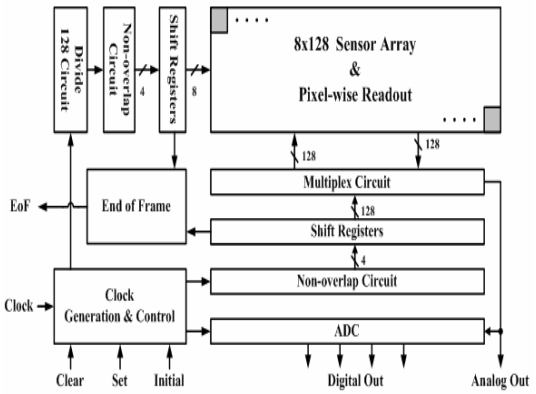


Fig. 3 Test chip architecture of 8x128 sensor array

Fingerprint acquisition is based on conventional capacitive sensing method, we develop an efficient capacitive sensor structure to improve the performance of readout circuits integrated in a unit pixel[1]. The sensor structure is illustrated in Figure 4. Sensor plate in unit pixel is composed of top metal layer (metal 4 is according to the technology we used).The capacitance (C_F) induced by fingerprint and the top metal layer is calculated to be about 0~150 fF. The next two lower metal layers, i.e. metal 3 and 2, are used to form two intermediate capacitors. The readout circuit can be directly implemented under the sensor plate. Three switches are placed between the power lines and the metal layers. There are two steps to describe the sensing operation. In the step 1, the capacitor C_F and C_B are separately charged by V_1 and V_2. In the meanwhile, the capacitor C_P is settled by difference between V_1 and V_2. In the step 2, the C_P is short-circuited while C_F and C_B are instantaneously connected to the output node (V_{Out}). The switch control signals are arranged by a two-phase non-overlapping clock. The output voltage can be computed by equation 1 as:

$$V_{Out} = \frac{V_1(C_F + C_{SW}) + V_2(C_B + C_{SW})}{C_F + C_B + 2C_{SW}} \quad \ldots\ldots (1)$$

, where C_{SW} is the parasitic capacitance of switches. If V_1 is given by V_{DD} and V_2 is 0 volt, so $V_{Out} = V_{DD}$ (C_F+C_{SW}) / $(C_F+C_B+2C_{SW})$. From equation 1, we can find out that parasitic capacitor C_P has no influence on the output voltage. Also the C_{SW}'s have only a little influence on the output voltage. Different switch sizes and parasitic capacitance value (C_P) have been performed by simulation. Only about 10 mV variation appears due to these non-ideal factors. Hence the output voltage may be simplified to $V_{Out} = V_{DD} C_F / (C_F+C_B)$. In other words, it is straight for the designer to only take care on the intermediate capacitance between the metal 3 and metal 2 (C_B). We can intentionally design the value of C_B by the layout or some other control scheme. By controlling the value of C_B for different range of C_F, the V_{Out} can be adjusted to a reasonable range for subsequent processing.

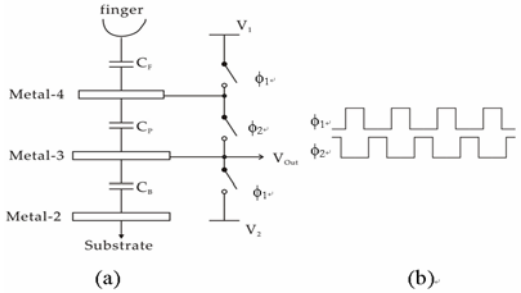


Fig. 4 (a) The proposed sensor structure, (b) Two-phase non-overlapping control signal

The complete schematic in a unit pixel is depicted in Figure 5. Four transistors make up the three switches of the proposed sensor structure. The PMOS transistor can pre-charge the top metal to VDD, while the NMOS reset metal 3 to ground. The transmission gate provides wide dynamic range for the captured voltage. By eliminating

1. USA patent pending

the two-phase non-overlapping clock, C_{SEL} and R_{SEL} signals are used to simply control these switches. C_{SEL} represents column select signal; otherwise R_{SEL} means row select signal. They are used for pixel-wise reading sequence, i.e. sensing data processed pixel by pixel. C_{SEL}* R_{SEL} is synthesized by an AND logic to achieve the pixel-wise reading scheme.

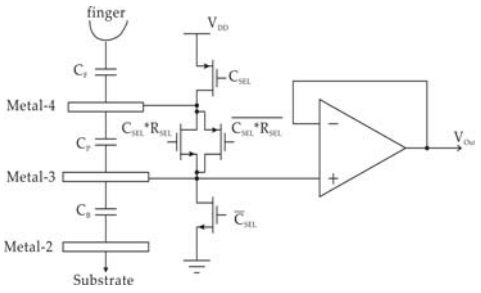


Fig. 5 Schematic of a unit pixel

In the unit pixel cell, a unity-gain buffer is used for the sensed V_{Out} to drive the parasitic capacitive load existed in the interconnection among the sensor array. It is necessary to put an analog buffer blocking the sensed output voltage from the back-end processing circuit to ensure the signal integrity. To consider the limited unit pixel area, it is not adequate to construct the buffer by complicated structure, so a simple differential amplifier is utilized as shown in Figure6. Differential pair (M1 and M2), current source (M6), and the current mirror load (M3 and M4) form the core amplifier. M5~M7 establish the simple diode-connected bias. When the pixel is not selected, M_{SW} cutting off the power path in the buffer can save the power consumption.

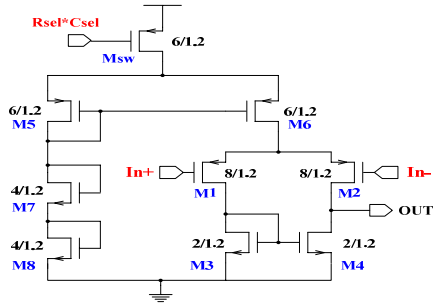


Fig. 6 Unit gain buffer used in pixel

Readout control signals, which include column and row select, are synthesized from logic gate, as shown in Figure 7. A clock input is needed to generate the desired column and row select signals, as shown in Figure 8. In order to simplify the reading scheme, we adopt the way of processing the fingerprint data one pixel at a time.

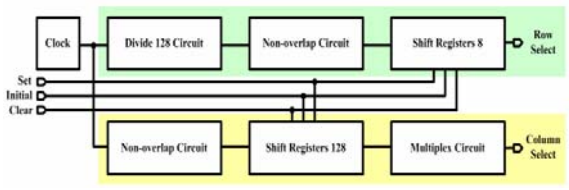


Fig. 7 Readout control signals

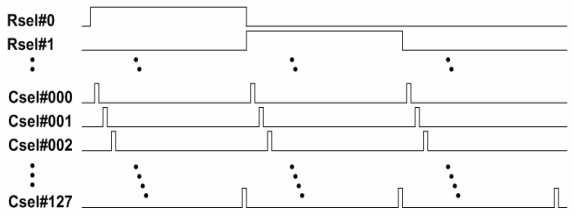
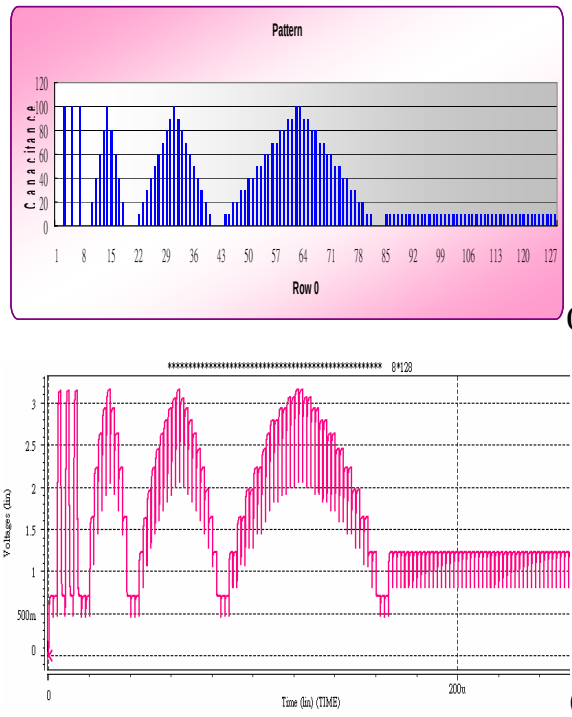


Fig. 8 Row select and column select signals

4: SIMULATION AND EXPERIMENT RESULTS

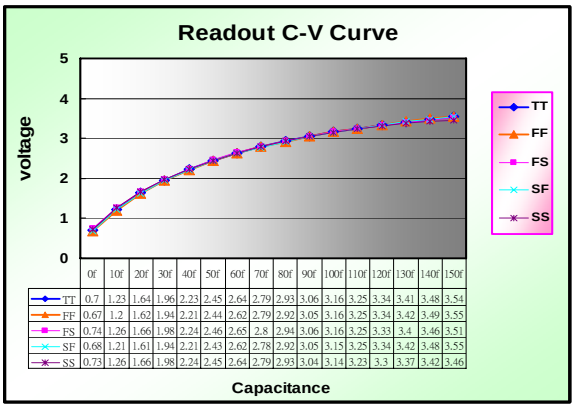
The chip of the 8 x 128 sensor array with readout circuits is simulated and fabricated by using TSMC 0.35-μm 2P4M 5V CMOS process. Figure 9 showed the simulation about the readout of a row array. In this case, we assume that the fingerprint sensor array was touched by finger, the capacity value will vary and reveal the result of readout circuits. The simulations of five corner cases on the output voltage versus sensed capacitance are summarized in Figure 10. The output voltages are ranging from 0.7V to 3.5V for C_B designed to be 50fF. It is sufficient for fingerprint acquisition. The characteristics of the chip are listed in Table 1. The unit pixel size is 50 x 50 μm^2 to achieve resolution of 500 dpi. The input clock rate is set to higher 500kHz to than have ten frames per second for an 8 x 128 array. The photograph of the chip is shown in Figure 11. The chip size is 7307.1 x 748 μm^2.



(a)

(b)

Fig.9 Sensor array simulation (a) offer different capacity values (b) and reveal the result of readout circuits.



	0f	10f	20f	30f	40f	50f	60f	70f	80f	90f	100f	110f	120f	130f	140f	150f
TT	0.7	1.23	1.64	1.96	2.23	2.45	2.64	2.79	2.93	3.06	3.16	3.25	3.34	3.41	3.48	3.54
FF	0.67	1.2	1.62	1.94	2.21	2.44	2.62	2.79	2.92	3.05	3.16	3.25	3.34	3.42	3.49	3.55
FS	0.74	1.26	1.66	1.98	2.24	2.46	2.65	2.8	2.94	3.06	3.16	3.25	3.33	3.4	3.46	3.51
SF	0.68	1.21	1.61	1.94	2.21	2.43	2.62	2.78	2.92	3.05	3.15	3.25	3.34	3.42	3.48	3.55
SS	0.73	1.26	1.66	1.98	2.24	2.45	2.64	2.79	2.93	3.04	3.14	3.23	3.3	3.37	3.42	3.46

Fig. 10 Simulations on sensed capacitance vs. voltage

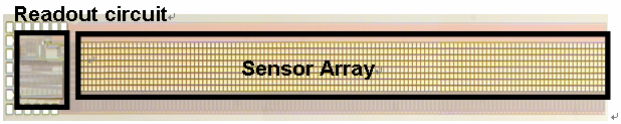


Fig. 11 Chip photograph

Table 1. Characteristics of the sensor

Technology	2P4M 0.35μm CMOS
Die size	7307.1 × 748 μm^2
Pixel size	50 × 50 μm^2
Voltage swing	0.7 ~ 3.5 Volt
Capacitor Range	0f~100f
Power supply	5 Volt
Clock rate	500kHz
Digital output	4 bits
Power Consumption	＜30mW

The measurement results are shown in from Figure 12 to Figure 15. Figure 12 shows the end-of-frame output signal, which has a pulse every 2048 clock cycles, to confirm the operation of readout control. Then we carefully put our finger approaching the sensor array as shown in Figure 13. The 4 bits of digital output are measured as in Figure 14. The measured data are transferred to a personal computer and plotted by Excel to show the 2D sensed image as shown in Figure 15. Figure 15(a) shows the one frame result, and Figure 15(b) shows the result of six consecutive frames.

The ridges and valleys of fingerprint can be clearly distinguished. The maximum induced capacitance measured is about 55fF. To summarize these experimental results, the fingerprint acquisition chip we proposed can capture the fingerprint adequately.

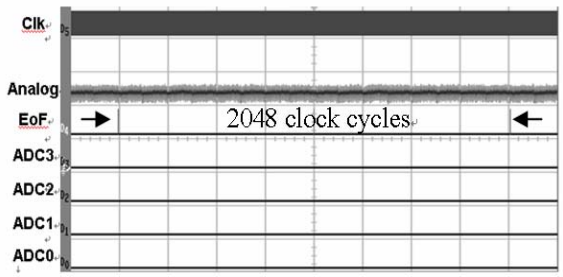


Fig. 12 End of frame signal

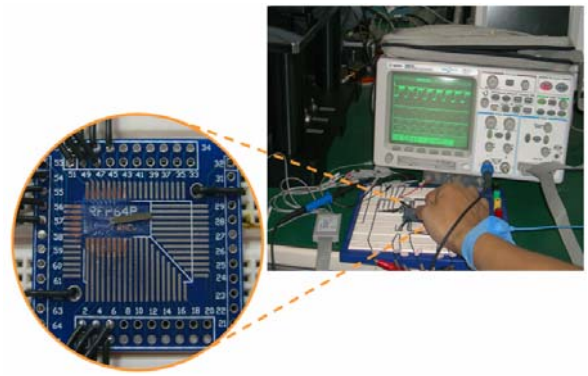


Fig. 13 Touched by fingerprint and test board

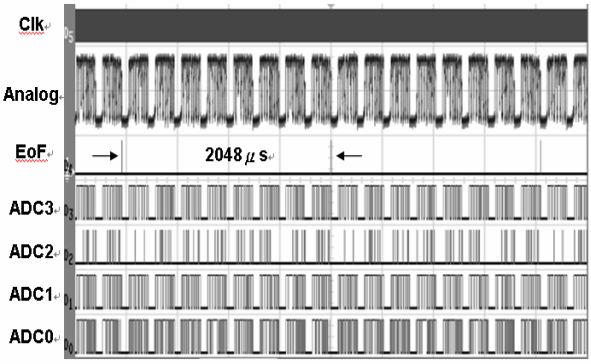
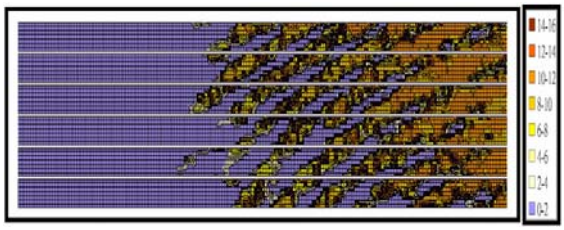


Fig. 14 The 4 bits of digital output codes

(a)



(b)

Fig. 15 The 2D image plot (a) one frame (b) six frames

5: CONCLUSION

A sweep capacitive fingerprint sensing chip is presented in this paper. With the insensitivity to the parasitic capacitance and its large output voltage range controlled by a designed intermediate capacitor, this method has been proven to work well on fingerprint acquisition. A test chip of 8 x 128 sensor array is designed and implemented by using a standard CMOS process. Simulation and measured results match well and confirm the performance of our proposed capacitive sensor structure and readout circuit.

Acknowledgment

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