A Low Power Flash Analog-to-Digital Converter Using Level-Detection Method

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ABSTRACT

In this paper, a new low power design method for flash Analog to Digital Converters(ADCs) is presented. As an example of 6-bit flash ADC, all comparators are divided into 8 regions. We use level-detection method to let only one region is working in every clock cycle, and then achieves the aim of low power consumption. Simulation results show that this proposed 6-bit flash ADC consumes about 37.8mW at 400Msample/s with 3.3V supply voltage in TSMC 0.35μm 2P4M process. Compared with the traditional flash ADC, our level-detection method can reduce about 69.1% in power consumption.

1. INTRODUCTIONS

Digital receivers for high-bit-rate communications are spurring on the conversion rate of ADCs. For example, the ADCs are used in hard-disk drive must guarantee high speed and low power. Hence the ADC plays an important role between analog and digital signals. Among all kinds of ADCs, because of the paralleled scheme of flash ADC can rise up the conversion rate, so it has the advantage with high speed conversion rate. However a high resolution flash ADC will cost very large chip area and high power consumption. The increasing demand for battery-operated device, low power consumption for portable devices are more popular and requires special attention to power consumption. Especially in SOC system, a low power consumption device has emerged as an important issue in the design of electronic circuit.

In the traditional flash ADC architectures[1-5], as shown in Fig. 1, we can find that all of comparators are working currently in every clock cycle, and cost high power consumption.

This paper introduces a new technique to save power consumption for flash ADCs. To overcome the high power consumption, we propose a level-detection design method and divide all comparators of n-bit flash ADC into several regions and let only one region is working in every clock cycle, and that can reduce the total power consumption.

The rest of this paper is organized as follows. In section2, the level-detection method is proposed to reduce the power consumption of flash ADCs. The overall scheme and the detailed method for the control circuit are shown in section2. Section3 shows the experimental results of the flash ADC which used the level-detection method. The power consumption for our proposed method is compared with other traditional flash ADCs. Conclusions are given in Section4.

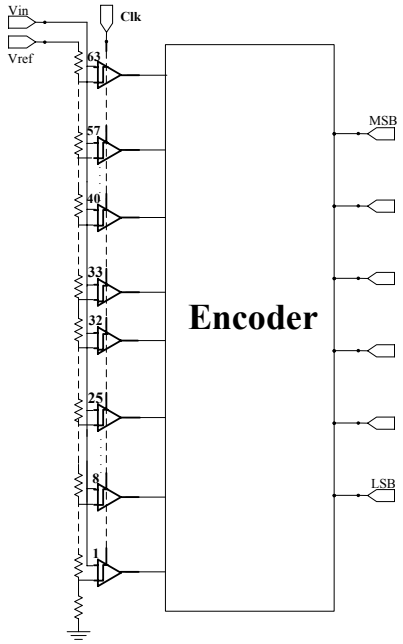

Fig. 1 Traditional flash ADC architecture

2. PROPOSED LEVEL-DETECTION FOR FLASH ADC

2.1 PRINCIPLE OF PROPOSED LEVEL-DETECTION METHOD

To reduce high power consumption of traditional flash ADC, we employ a new level-detection method to detect where the input signal voltage intervenes and let only one selected region work. It is like when we read the degrees of the thermometer; we only care about the level of the mercury. When the magnitude of input signal lies between a specific range, control circuit will make the corresponding region work, the other regions are not. As an example of 6-bit flash ADC, we divide 63 comparators into 8 regions. As shown in Fig. 2, when the input signal is greater than V_{ref33} and less than V_{ref41}, only region5 is working, the others are not. To implement this idea, we divide 63 comparators into 8 regions, and generate fifteen control signals to select the

corresponding working region. The architecture of our proposed ADC is shown in Fig. 3.

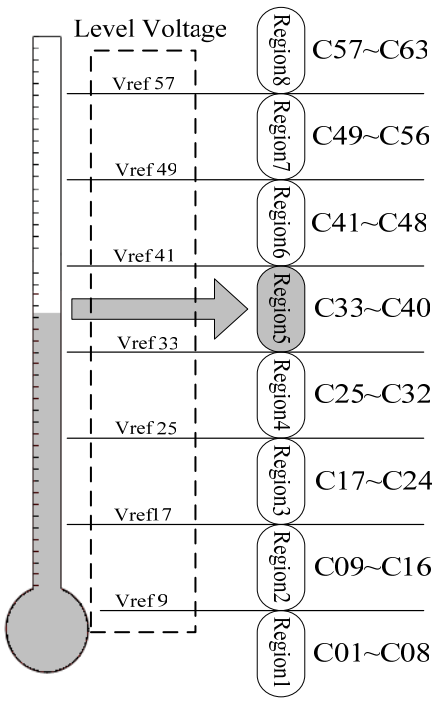

Fig. 2 Level-detection for 6-bit flash ADC

2.2 CONTROL CIRCUIT OF LEVEL -DETECTION

As we known, comparator plays an very important role in flash ADC. In order to save the power consumption, we adopt a low power comparator[6], as shown in Fig. 4.

The characteristic of the low power comparator, when $V_{in} > V_{ref}$, the output of V_{out+} is high, and the output of V_{out-} is low. On the contrast, when $V_{in} < V_{ref}$, the output of V_{out+} is low, and the output of V_{out-} is high. With this characteristic we mention above, we use the low power comparator to detect where the input signal intervenes.

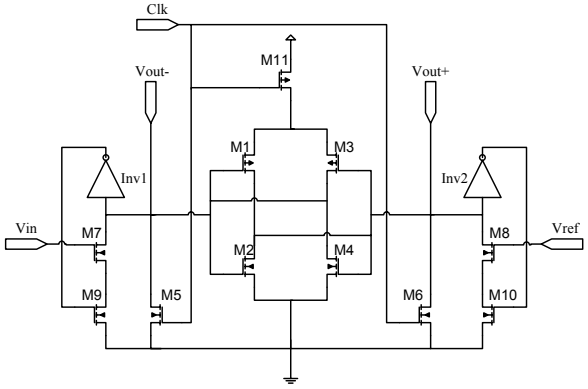

Fig. 4 Low power comparator used in proposed method

The level-detection control circuit of 6-bit flash ADC is shown in Fig. 5. Basically, it is composed of seven comparator and some logic gates. The connection of region-selection signal for flash ADC as shown in Fig. 3.

For example, when $V_{in} > V_{ref41}$ and $V_{in} < V_{ref49}$, the L6- of L6 and the L5+ of L5 will be high, we can obtain the region-selection signal from the output of the AND gate, as shown in Fig. 5. That is to say, only region6 is working and the others are not. Because the low power comparator only working when the clock signal is low, we need to add a NOT gate. When region6 is working, the S7_6 and S6_5 will generate region-selection signal, too. Not only the C41~C48 are working, but also C39, C40, C49 and C50 are working.

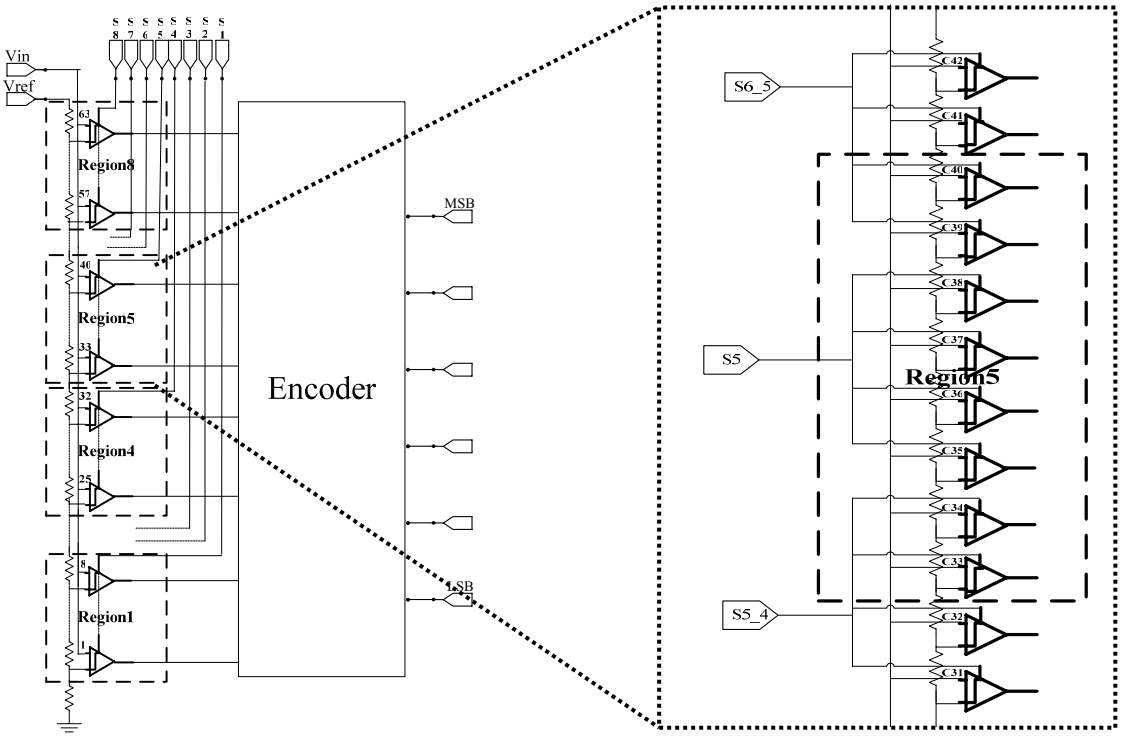

Fig. 3 Architecture of proposed flash ADC

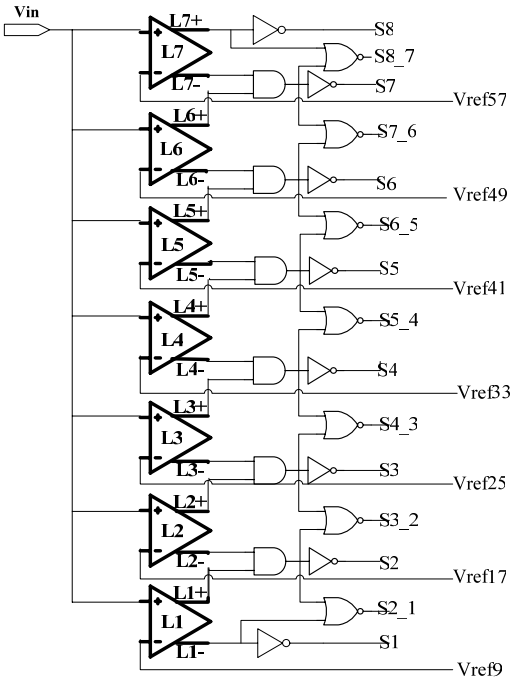

Fig. 5 Control circuit for level-detection method

Suppose the input signal is equal to V_{ref41} If the control circuit selects region5, then the C31~C42 are working. If the control circuit selects region6, then the C39~C50 are working. No matter how the control circuit selects the region5 or region6, the C39, C40, C41 and C42 are still working. Under this design, it won't output incorrect result although the control circuit selects the wrong region, as shown in Fig. 6.

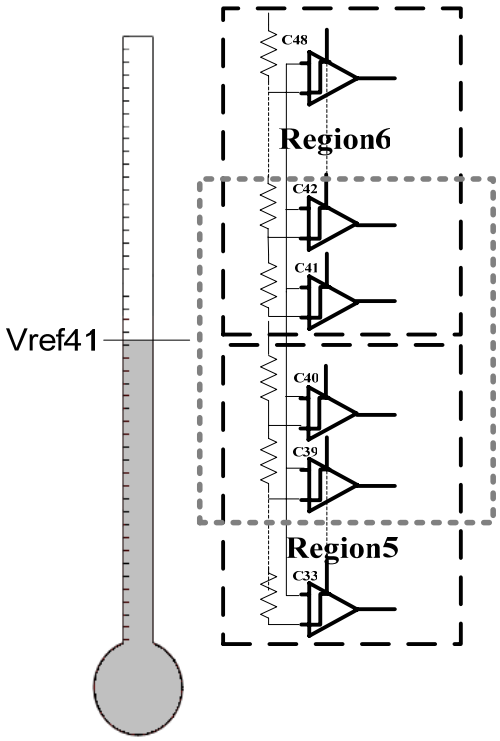

Fig. 6 A illustration of the control circuit meet meta-stability

3. SIMULATION RESULTS

Fig. 7 and Fig. 8 show the simulations of the control circuit and our proposed 6-bit flash ADC, simulation condition: input ramp signal which voltage range is form 0 to 2V for proposed 6-bit flash ADC and control circuit, reference voltage 2V, power supply 3.3V, sampling rate at 400MHz. The control signal shows that there are only one region and the nearby comparators are working.

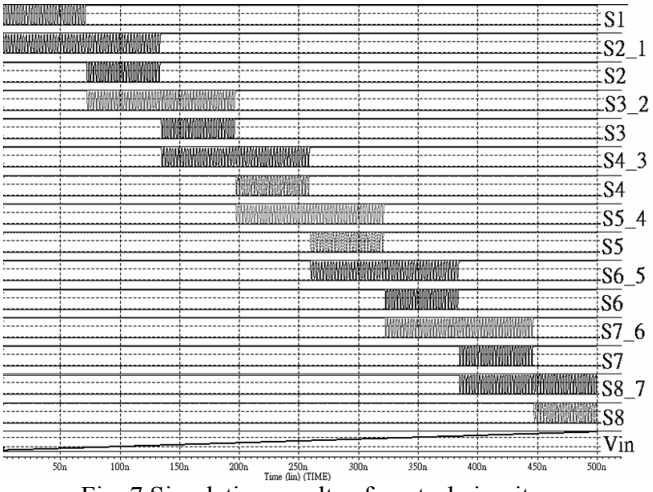

Fig. 7 Simulation results of control circuit

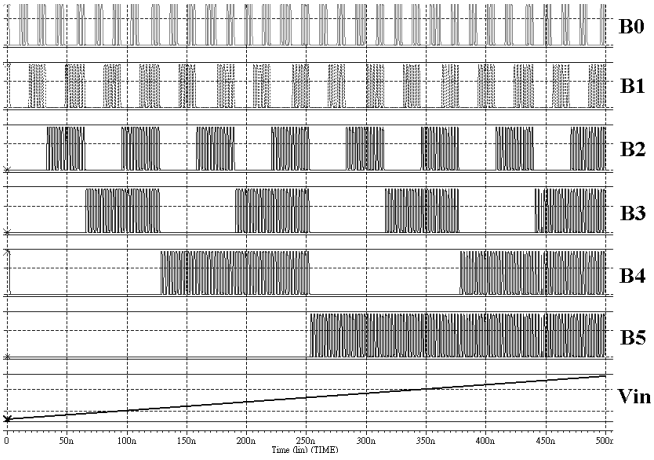

Fig. 8 Simulation results of proposed 6-bit flash ADC with level-detection method

To compare the power consumption among traditional 6-bit flash ADC, bi-section method[7] and our proposed method, we have simulated each circuit with HSPICE in TSMC 0.35μm technology. The simulation results are made in the same condition, input sine-wave signal which operates at 10MHz along with V_{p-p}=2V, reference voltage 2V, power supply 3.3V, sampling rate at 400MHz. Table 1 shows the power consumption comparisons of each flash ADC. The power consumptions are 122.52mW, 82.49mW and 37.80mW for traditional method, bi-section method and our proposed flash ADC, respectively. We can save power dissipation up to 69.1% and 54.2% compared to

traditional method and bi-section method[7]. The DNL is with in 0.2LSB/-0.8LSB, the INL is within 1 LSB/-0.3LSB. Finally, we have designed a 6-bit flash ADC with level-detection method in TSMC 0.35µm 2P4M technology. Fig. 9 shows the layout of our proposed flash ADC. The chip area occupies $1.13*1.13mm^2$ with I/O Pads. The specifications of our proposed flash ADC are shown in Table 2.

Table 1 Comparisons of power consumption

Architecture / Spec.	Traditional	Bi-section	Proposed
Technology	TSMC /0.35µm	TSMC /0.35µm	TSMC /0.35µm
Power Supply	3.3V	3.3V	3.3V
Resolution	6 bits	6 bits	6 bits
Input Analog Range	0~2V	0~2V	0~2V
Power Consumption @100MHz	60.86mW	44.48mW	19.20mW
Power Consumption @200MHz	85.76mW	65.00mW	25.56mW
Power Consumption @400MHz	122.52mW	82.49mW	37.80mW

Table 2 Specifications of proposed flash ADC

Resolution	6 bits
Technology	TSMC/0.35µm
Power Supply	3.3V
Reference Voltage	2V
Input Range	0~2V
Sample Rate	400MHz
INL	0.2LSB/-0.8LSB
DNL	1 LSB/-0.3LSB
Power Consumption	37.80mW
Chip Area(With Pads)	$1.13*1.13mm^2$

4. CONCLUSION

This paper presents a new low power design for flash ADC. With the simulation results, our proposed level-detection method can save the power consumption about 69.1% than traditional method and about 54.2% than bi-selection method. The DNL of our proposed flash ADC is within 0.2LSB/-0.8LSB, and the INL is within 1 LSB/-0.3LSB. The results approve proposed level-detection method can reduce the power consumption for a flash ADC effectively.

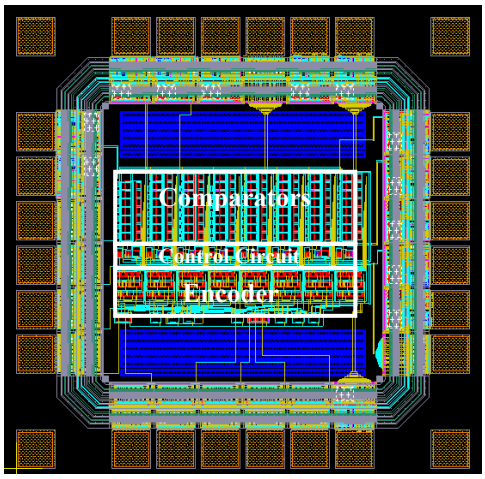

Fig. 9 Layout of proposed 6-bit flash ADC

5. ACKNOWLEDGEMENT

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